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Advanced Semiconductor Technology and Plasma Processes

次世代デバイス開発とプラズマプロセス

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Continuous shrinking of MOSFETs (MOS Field Effect Transistors) has enabled to realize 90nm technology node LSI, in which the transistor gate length ranges from 37 to 65nm and will be further scaled down to 18 to 25nm at 45 nm mode in 2010.

Aggressive scaling of MOSFETs induces a significant increase of leakage current through gate dielectrics when conventional gate oxides are employed (Fig.1). To avoid the exponential rise of power consumption due to the gate leakage current, a new gate insulator with a high dielectric constant (high-k) must be developed for replacing the conventional gate oxides. Also, for enhancing the MOSFET drive current, the poly-Si gate needs to be replaced by metal gate. The other important approach to achieve higher performances of MOSFETs is to employ new channel materials with high carrier mobilities or new channel structures.

As illustrated in Fig. 1, the basic transistor structure remains unchanged, while the materials in the active region are dramatically changed in the near future.

The signal propagation delay or RC delay through metal interconnects, which limits the integrated circuit performance, is also a big concern. To minimize the RC delay and reduce the power consumption, the interlayer dielectrics such as conventional SiO_2 must be replaced by low dielectric constant (low-k) materials ($k<2.5$). Thus, many of plasma process technologies so far developed for fabrication of integrated circuits can not be directly applied to such new materials.

This paper reviews recent progress and future prospect of semiconductor technology, by highlighting the plasma processes which certainly continue to play crucial roles.

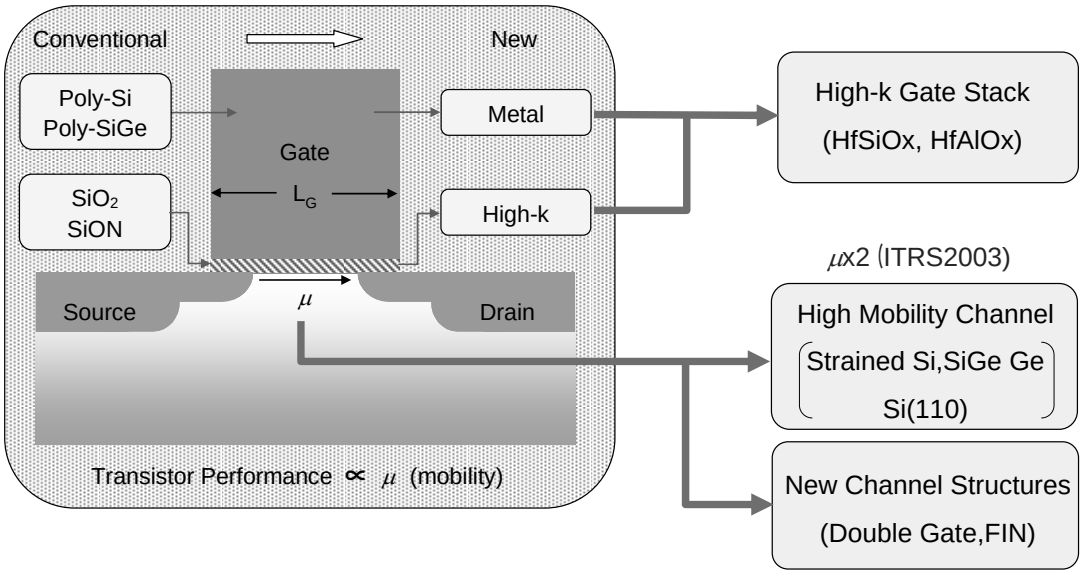

Fig 1. Cross sectional view of an MOS transistor with a conventional poly-Si gate/SiO_2 or SiON structure and a new metal/high-k gate stack. For enhancing the transistor performance, high mobility channel materials or new channel structures are being developed.