

Simultaneous Measurement of Coarse and Unscheduled Rapidly Changing Plasma Parameters during Long Pulse Discharges

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Abstract

In a long pulse discharge plasma parameters changes rapidly because of unpredictable unknown events. These unpredictable rapid changes in plasma parameters should be examined in detail in order to understand the properties of plasma. Normally the unknown events causes a fast changes in plasma parameters and to capture these rapid changes one need to change the sampling rate from the normal sampling rate. This requires to digitize the plasma parameters at two different sampling rate, one at slow sampling rate during the low activity period and another at fast sampling rate to capture the changes occurring at the time of unknown events. This demands for simultaneous coarse and unscheduled rapid change measurement of plasma parameters at different sampling rates. To fulfill above requirement a CAMAC digitizer module has been designed to acquire the data for the whole shot at one sampling rate and to capture the unscheduled rapid changes at higher sampling rate simultaneously. The module is capable of detecting unknown event and changes the sampling rate by ten times for rapid changes measurements. It can store 16 K samples for fast events and 32 K samples for whole shot duration. Besides, the module has some other important features, different modes of operation, a monitoring mode, a single shot mode (Pre/Post trigger acquisition) with selectable sampling rate upto 1 MHz and a lossless continuous acquisition mode. The module was tested for 1 kHz nominal sampling rate for 3.2 seconds data and 10 kHz at the time of event occurrence for 160 msec. data. with 8 K pre trigger samples.

Keywords:

CAMAC, data acquisition, steady state, digitizer

1. Requirements Involved in long Pulse Digitizers

Nowadays, because of the advent of continuous measuring, multi-channel diagnostics and elongation of pulse duration, the data volume has grown excessively high. Acquisition and storage of data at high rate is neither practical for technical reasons, nor necessary because much of data does not contribute to better insight into the observed phenomena. Data acquisition design should therefore develop methods to acquire or keep only the data that are required for scientific

research.

Specifically the data management due to large amount of data generated by experiment will be very crucial. The devices with long pulses or continuous running device requires, a fundamentally different type of digitizers. The important difference between pulsed and near steady state operation of acquisition system will be in the acquisition technique of signals. In the case of pulsed operation, the most common way is to acquire data and store it in a local storage. But the same

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concept cannot be adopted for steady state devices since it would lead to a very large size of dual ported data storage elements on the digitizer. A more suitable approach would be event-based acquisition. In such an approach most of the time data are acquired at a relatively lower sampling rate during low activity period, but when a given event occurs, acquisition-sampling rate is increased to a level fast enough to extract the maximum information for a limited period. The demand placed on instrumentation is considerable in case of event driven sampling based data acquisition. It will require a system that can deal with continuous flow of events as well as event detection and distribution systems.

For not losing any physics information during shot, all digitizers have to be ready to sample data at required highest rate, to detect the event and to change sampling rate when event takes place. This ensures no loss of any physics information. The digitizer system should automatically recognise when it is necessary to begin taking data, so that data can be continuously taken and archived until the pulse ends. The local front-end storage facilities should accommodate and manage this voluminous acquired data. Further, the embedded intelligence should determine whether to increase or decrease the sampling rate depending upon the experimental status to take care of any schedule or unscheduled events.

Most of the available digitizers in CAMAC do not support for simultaneous reading and writing of data. Either the module is in the digitization mode or in a computer read out mode. Hence it can not support lossless continuous acquisition. Moreover it does not have any event detection hardware on board. It has a very limited local storage and hence cannot support high sampling rate for a long time. Limited storage compels one to restrict the sampling rate to value low enough to accommodate the entire shot. Hence one loses the high frequency component which may originate from unscheduled events. The scheme described below address these issues.

2. Hardware Description

The designed CAMAC digitizer consists of two data storage elements for storing the data at two different sampling rates. The first one uses a FIFO (first in first out memory), stores the data at faster sampling rate. Another, which is a RAM memory, stores data at slower sampling rate for coarse measurements. Sampling rate for detailed measurements and coarse

measurement can be selected by CAMAC commands.

The available sampling rate is from 0.1 Hz to 1 MHz. A sampling clock that has been selected for detailed measurements is divided further and used as a sampling clock for coarse measurements. The analogue signal is digitized at a fast sampling rate and digitized data is first placed in the FIFO buffer. FIFO is read out at same rate after taking the pre trigger data.

The data read out from FIFO are stored in the RAM memory at selected coarse sampling rate. e.g. if the sampling rate for 100 kHz is selected for detail measurements and 10 kHz has been selected for coarse measurements, then in FIFO every sample at 100 kHz is stored and every tenth read out from the FIFO is stored into the RAM buffer for long term storage. Saving data into the RAM buffer is started after taking the pre trigger data. Once the acquisition is started with start trigger, the acquisition can be stopped by stop trigger pulse.

The stop trigger is generated on detection of fast event. On receiving the stop trigger the FIFO storage contains the data at 100 kHz for last (10 micro sec \times 16 K) 160 milli sec. And RAM contains coarse data for (100 micro sec \times 32 K) 3.2 seconds.

2.1 Block diagram

The block diagram Fig. 1 shows how various elements are internally connected to various buses for achieving the described features.

- CAMAC access to program various registers
- Transfers of data from ADC to FIFO and RAM memory.
- Transfers from Memory to CAMAC data way
- Clock Generation.

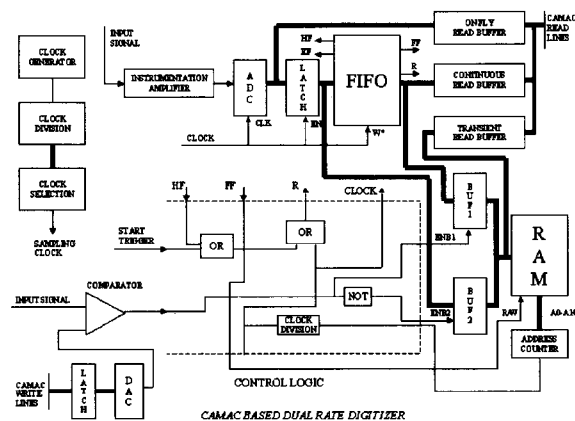


Fig. 1 Block Diagram

- CAMAC function decoding.
- Control Logic Generation

2.1.1 Clock generation

The master oscillator is running continuously and is generated using a 10 MHz crystal. For sampling clock this basic clock is further divided by various stages of counter. Multiplexer selects the required fast sampling clock via CAMAC commands. The same clock is further divided by ten for slow sampling rate.

2.1.2 ADC

The selected ADC is flash type 8 bit ADC. It has built-in reference voltage source and sample & hold circuits. The selected sample rate clock is applied to start conversion for digitizing the analogue signal. The digitized data is latched and made available to CAMAC data bus for on fly read out as well as to FIFO for data storage.

2.1.3 FIFO buffer

The FIFO (first in first out) type of memory supports simultaneous reading and writing to it. The continuous lossless acquisition is made possible because of this feature. Initially the FIFO is reset by CAMAC init. command F9. Once the digitization is started, by F28 CAMAC command, digitized data is written to FIFO on every sample clock. Once the Half-Full (HF) flag is set, the same clock is applied to read out the FIFO and FIFO enters into a dummy read out mode. The HF is used for LAM generation in continuous acquisition mode. This is continued till the start trigger is applied externally or by software F25 command. On receipt of start trigger, the data transfer to RAM memory starts. This goes on till the stop trigger is received. On receipt of stop trigger the FIFO stops reading out and stores the data till full flag is generated.

2.1.4 RAM buffer

Data for the entire shot is stored in 8 Bit by 32 Kbytes read/write memory. With initialization on F9 command this module goes into the write mode and all address generation counters are set to zero pointing at first location of memory. The data read out from FIFO after the receipt of the start trigger is stored into the memory. The address generation logic increments address on every sampling clock selected for coarse sampling measurements. On receipt of stop trigger it continues storing data till the full flag of FIFO stops the clock.

2.1.5 Stop trigger generation

To detect the fast event a comparator and a DAC are used. The analog signal is compared with a threshold generated by DAC and generates the stop trigger. During the initialization of module, a required number is loaded to DAC latch for generating required DC threshold.

2.1.6 Control logic and timing

The required logic for controlling various elements is generated using gates, flip-flops and sequential circuits.

3. Application Software

A user friendly software has been developed using Lab/Windows CVI which provides a graphical panel to the user for different modes of operation. The module can be utilized in various operating modes. With the help of control panel user can select various modes of operation, configure the module, plot the data points and can make the hard copies of plots. Figure 2 shows data acquired in a single shot mode and control panel for various modes of operation. Figure 3 shows data acquisition with event. The first plot shows the complete 32 K data points stored in RAM memory which is taken at 1 kHz sampling rate. Second plot shows the selected 4 K data points of shot. While third plot shows the data from the FIFO around the event occurrence with more details which has been taken at 100 Hz sampling rate.

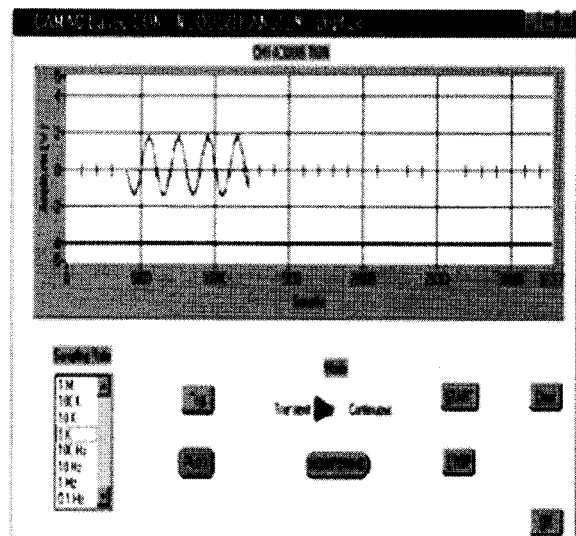


Fig. 2 Data in single shot mode

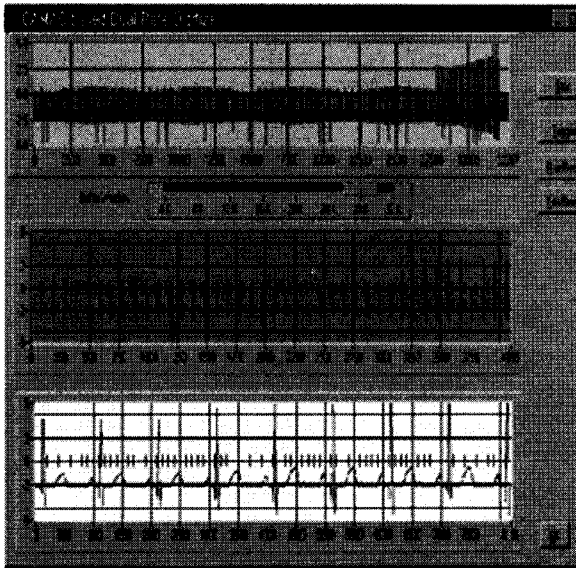


Fig. 3 Event capturing in single shot mode

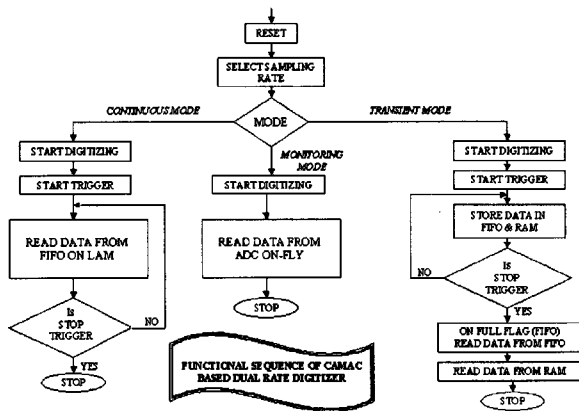


Fig. 4 Sequence of operations in different modes of operation

3.1 Operating modes

The module can be operated in three different modes. Single shot with dual sampling, capturing the event. Monitoring mode for long term monitoring by reading the current ADC data value. Continuous acquisition mode where transfer of data from FIFO buffer to host takes on half-full flag. Figure 4 shows the flow diagram and operation sequence for deferent mode of operation.

4. Summary

The digitizer was tested with various different kinds of signals and operated in all deferent modes. The events were generated to by varying the amplitude by programming the arbitrary waveform generator. The plots of acquired signals clearly shows finer details of waveform obtained in FIFO buffer whereas the plots of RAM buffer which takes at ten times slower sampling rate to accommodate entire shot. One of the most significant advantage of the module is that it captures entire shot at slower sampling rate, ten times faster sapling rate around event for detailed data, on board event detection with polarity and magnitude, everything in single module.

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