

## Challenges of leading-edge technology in plasma processing

### 先端プラズマプロセス技術の課題と展望 1

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Dimensions of semiconductor devices shrink into nanometer range. In this area, more accurate surface reaction control is required in plasma etching. Time modulation (TM) of discharge and gas injection was investigated to improve etched profile. It was found that etched profile (vertical, selectivity, wiggling) was improved in critical etching process. Integrated process tool with PE-CVD was investigated for MRAM patterning. It was found that deposition and oxidation were suppressed at the sidewall.

### 1. Introduction

As dimensions of semiconductor devices shrink further into nanometer range, transistor performance is improved not only by scaling and adopting boosting technology but also by adopting new channel material and structure. It is also required to reduce power consumption in mobile devices. In logic devices, 3D-transistor (FinFET) was adopted to improve switching property. Also, stacked Flash memory cells (3D-NAND) and non-volatile memory (e.g. MRAM) are investigated to replace a portion of current memory devices. When fabricating these devices, more accurate and higher aspect ratio patterning is required. For example, in logic device fabrication, fin width reaches 3.7 nm at the 5nm node, where nanowire FET and Ge/III-V channel materials are other candidates [1]. Thus, required accuracy will reach atomic level in the etching process. To realize nm scale etching, new etching process functions are necessary to suppress wiggling, roughening, and degradation of etched layer as well as improve selectivity. At the same time, reasonable productivity (through-put, stability, repeatability) is required for mass production. In the 90's some sophisticated functions were already investigated such as pulsing control, atomic layer control, *etc.*, [2-8] however were not adopted at that time. As devices shrink these functions seems to become useful.

In addition, etching of new material is required in emerging devices. For MRAM fabrication, not only reduction of deposition at sidewall of pattern in etching, but also encapsulation under vacuum is required to reduce degradation at the interface.

To meet these requirements, plasma etch tool was improved continuously. In particular, time modulation (pulsing of RF bias, discharge, and

gas) technologies and power control of wafer RF bias seems to be key technologies for accurate profile control as well as a selection of gas chemistry.

In this paper, we investigated time modulation (pulsing) technologies in directed self-assembling (DSA) mask etching and fin etching. Also this paper showed integrated process including etching and PE-CVD for MRAM patterning.

### 2. Time Modulation (TM) Technology

To improve trade-off between selectivity and etch profile, including iso-dense differences, TM (pulsing) technologies were investigated. TM bias (wafer RF bias pulsing) technology has already been used in semiconductor fabrication [7]. In nm scale etching, pulsed discharge and gas pulsing technologies [2] are candidates to improve etched profile.

Fig. 1 shows schematic view of microwave ECR etching apparatus and pulsing technologies (DTM: Dual Time-Modulation) [9]. Here, ECR

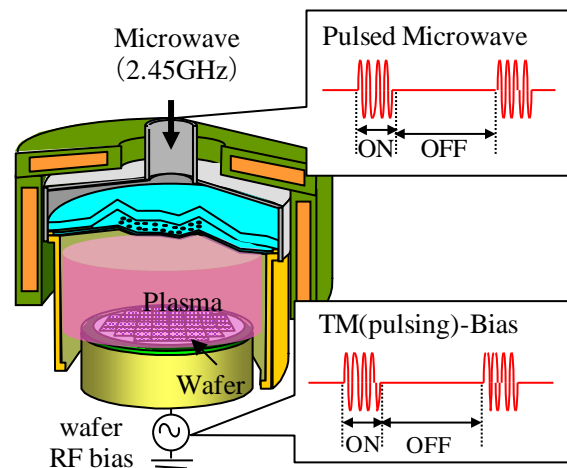


Fig. 1. Schematic view of microwave ECR etching apparatus and DTM .

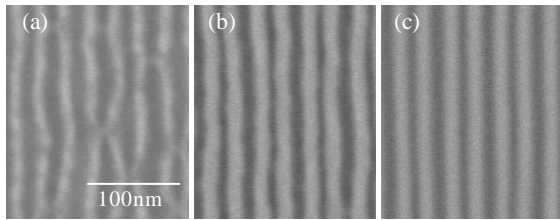


Fig. 2 Top view image after DSA mask etching.

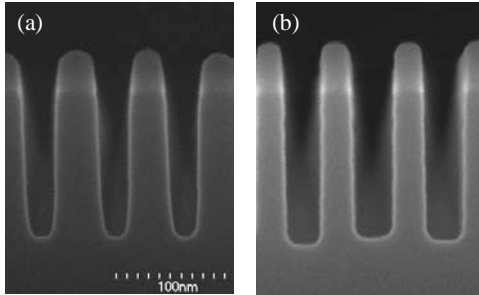


Fig. 3. Cross sectional SEM image after fin etching.

plasma was designed to have good affinity to pulsing discharge. By using the DTM, wiggling reduction was investigated in DSA mask etching. As shown in Fig. 2 (a), wiggling occurred in a continuous wave (CW) plasma. On the contrary, wiggling was improved dramatically by using DTM technology (b). Here, O<sub>2</sub> gas flow was adjusted to similar etching rate as (a). Finally, it was found that wiggling was eliminated without decreasing of etch rate (c). By using DTM, ion incident flux and activated O radical flux are suppressed even at low gas pressure condition. We considered wiggling was improved because the stress of the polystyrene surface did not increase.

Gas pulsing technology was investigated for fin etching [10]. Etching progress and sidewall protection steps were changed cyclically without interruption of the discharge. As shown in Fig. 3, etched profile using gas pulsing (b) is more vertical than that of continuous mixed gas injection (a). In addition, thickness of remained hard mask and etch front flatness were also improved.

### 3. Etching Technology for Non-volatile material

EMCP (Electro-Magnetically Coupled Plasma) etch tool was designed to enable long-term stability for non-volatile materials etching [11]. MRAM etching was investigated by using EMCP because typical MTJ etch by-products of Fe and Co are non-volatile.

In MTJ-MRAM etching, sidewall control is required to avoid chemical degradation of magnetic properties and to remove conductive deposition which causes electrical short. In addition, the MTJ seems to be degraded by air-exposure after etching. To overcome these issues the process tool was

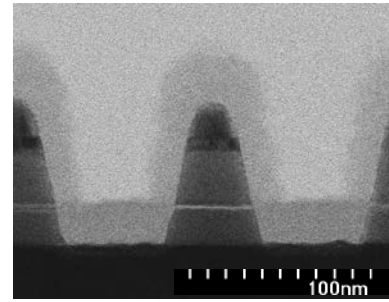


Fig. 4 Cross-sectional TEM image of MRAM etching.

developed with an integrated PE-CVD to encapsulate the etched profile under vacuum.

Fig. 4 shows cross-sectional TEM image of etching and encapsulation. Here, MTJ stack contained Ta electrode at the top and bottom. Taper angle was about 80 deg. Deposition and oxidation were not found at the sidewall due to suitable gas chemistry.

### 4. Summary

Plasma etching technology has been widely used in VLSI fabrication. This technology has been innovated by adopting new functions although some functions were proposed in 90's. In this paper, TM (pulsing) technologies (pulsed discharge and gas pulsing) were usable functions for nm scale device fabrication. For MRAM etching, a clean sidewall was achieved by using a specialized etch tool with under-vacuum encapsulation.

Atomic level precision etching is required in future device fabrication where etched material, etch stop layer, and structure become more complicated. Accurate surface reaction, reduction of stress and damage (both of physical and chemical) with reasonable throughput is required continuously in dry etching process. In addition, wet cleaning less after etching may be required as shown in MRAM patterning because removal of sacrifice layer becomes not acceptable or difficult.

### References

- [1] ITRS 2013.
- [2] K. Tsujimoto *et al.*, Proc. DPS, p.30 (1986).
- [3] S.Samukawa *et al.*, APL **63**, 2044 (1993).
- [4] N. Kofuji *et al.*, Proc. DPS, p.39 (1995).
- [5] T.Ono *et al.*, JJAP. **38**, 5292 (1999).
- [6] H. Sakaue *et al.*, JJAP. **29**, 2648 (1990).
- [7] T. Sugiyama *et al.*, Appl. Surf. Sci. **112**, 187 (1997).
- [8] H. Nishino *et al.*, JAP. **74**, 1345 (1993).
- [9] M. Morimoto *et al.*, SPIE 2014 [9054-18]
- [10] M. Tanaka *et al.*, JSAP Autumn meeting, 19p-S10-7, 2014.
- [11] M. Edamura *et al.*, Proc. DPS, p.87 (2002).