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Plasma Processes for Devices with New Materials to Reduce Power Consumption

新材料デバイスのプラズマプロセス
～ 消費電力低減を目指して ～

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This paper describes about recent technological challenges in the plasma processes for “Silicon Photonics” and “Spintronics”. Both of them are aimed to realize low-power-consumption devices.

1. Introduction

Low-power-consumption systems are now expected to realize low-carbon society [1]. For this purpose, two types of devices are receiving much attention due to their high-density, high-speed operation features for information processing and transmission. One is silicon photonics devices which are integrated devices of photonic/electronic functional-elements into one chip, and the other is spintronic devices which use non-volatile magnetic-tunnel-junction (MTJ) for information storage.

Silicon photonics was proposed for about 20 years ago, and it comes to a realistic devices aiming to replace conventional electrical wiring in a LSI chip, between board to board, and between server to server to optical interconnects [2]. This technology can reduce equipment size, widen bandwidth of communication, and realize low power consumption systems with low cost. On the other hand, 64 Mb MRAM was announced as a typical leading edge spintronic technology application [3]. It uses spin-transfer-torque technique to change the magnetization direction in the MTJ to overwrite the information. Even nonvolatile logic processor core using a three terminal MTJ cell was also demonstrated [4, 5].

2. Impacts of plasma processes in fabricating silicon photonic and spintronic devices

Important advantage to fabricate these devices is high compatibility of their special processes with CMOS processes. An example of a silicon photonic device is shown in Fig. 1. Optical waveguides (WG) are fabricated on SOI wafers with thick (~3 μm) buried oxide (BOX) layer [6]. A pedestal structure to embed a laser diode (LD) is fabricated by deep-Si/SiO_2 etching technique. Dot patterns of epitaxial Ge film is grown selectively on the Si-WG to receive modulated optical signals [7]. As shown here, the silicon photonic devices require wide variety of process technologies used in LSI fabrication. On the other hand, the MTJs used in the spintronic devices are placed between two interconnect layers of LSIs as shown in Fig. 2 [8]. The MTJs consist of three layers with nanometer-order thickness. Dry etching technique to fabricate the MTJs without causing damages on the device performances are a key issue. This paper describes current plasma technologies to fabricate these two types of promising devices.

3. Application of the plasma process

3.1. Si-WG with low line-edge-roughness (LER)

One of the most important issue to integrate silicon photonic devices is achieving ultra-low LER of the optical Si-WG. This is because, the LER of the WG is the primary degradation cause of laser light propagation. Theoretically, the propagation loss is proportional to the LER^2 [9]. Si gate process has similar LER requirements, and it uses low-LER lithography technique and anisotropic Si etching with ICP plasma. Thus, they are adopted to fabricate the low-loss WG. The LER of the WG evaluated by 3D-AFM was lower than 2.7 nm as shown in Fig. 3 [10, 11]. The propagation loss was less than 0.5 dB/cm which is the world record value among the silicon photonic devices at present, as shown in Fig. 4 [12].

3.2. MTJ etching with C-O based chemistry, and reductive damage-recovery treatment

C-O(X)-based chemistries such as NH_3/CO [13], CH_3OH [14], and their rare-gas dilution chemistries [5, 15] have widely been used since they proposed. These chemistries show high etch-selectivity between Ta hard-mask and the magnetic materials. Nature of the high etch selectivity is coming from a low etch rate of oxidized-Ta surface formed rapidly by chemical reaction with oxygen in the plasmas. Typical etched pattern shape is shown in Fig. 5 [16]. However, degradations of device performances by oxidation of magnetic materials are major issue in these chemistries [15]. To overcome the issue, recovery treatments by reductive plasma were proposed [17, 18]. Figure 6 showed the tunnel-magneto-resistance (TMR) ratio distributions over 300 mm wafers of a stacked CoFeB/MgO based MTJ before and after 150s of He/H_2 plasma treatment [18]. It clearly shows the TMR ratio recovery effect by this reductive treatment.

5. Conclusions

Important plasma processes to fabricate silicon photonic devices as well as spintronic devices were described. Evaluating actual device performances such as the propagation loss for the silicon photonic devices and the TMR ratio for the spintronic devices are the key when developing a new process technology. Tight communication between device side and equipment side is highly recommended.

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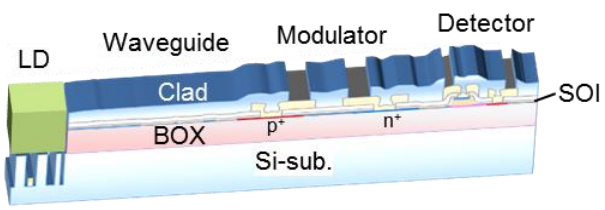

Figure 1 Cross sectional drawing of a typical silicon photonic device [12]. It is fabricated with using specially designed SOI wafer for the silicon photonics. Actual device includes high-speed RF electrical wiring (not shown here) to handle information electrically. Embedding many types of elements into one chip is one of the characteristics of this device.

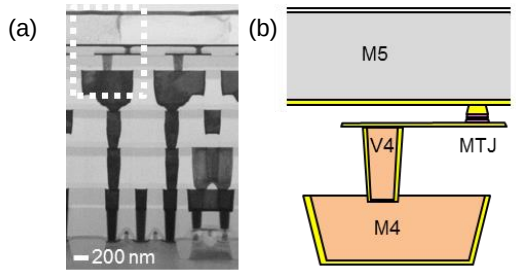

Figure 2 (a) Cross sectional TEM photograph of the spintronic devices with MTJ, and (b) enlarged schematic illustration of the part indicated by the rectangular dot on (a) [8].

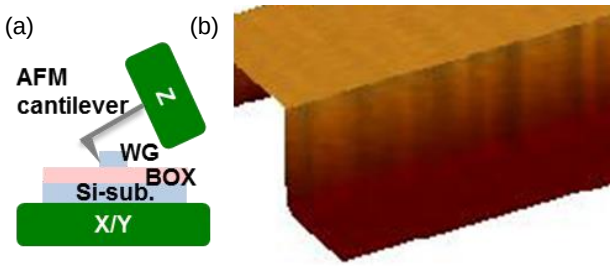

Figure 3 (a) Schematic illustration of 3D-AFM system, and (b) 3D-AFM image of Si-WG [11].

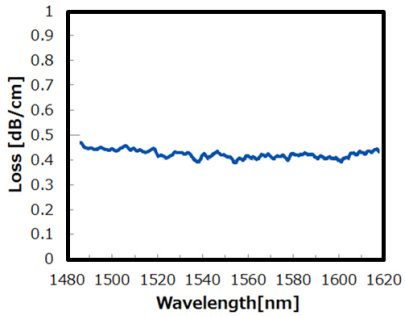

Figure 4 Propagation loss of TE mode as a function of wavelength [12]. The Si-WG was fabricated with using an immersion-ArF lithography technique.

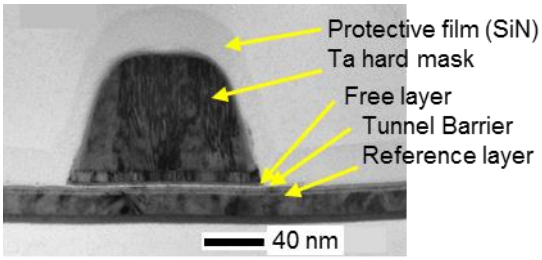

Figure 5 Cross sectional TEM image of a MTJ etched by Ar/NH_3/CO gas system [16].

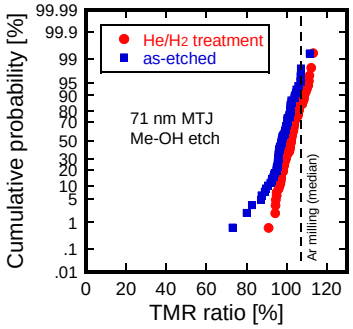

Figure 6 TMR ratio distributions of the 71 nm MTJ over the as-etched and the He/H_2-plasma-treated 300 mm wafers [18]. Median TMR ratio obtained from a small sample fabricated with Ar milling is also indicated by the broken line.