Plasma Process-Induced Damage in Microelectronics Fabrication
プラズマ誘起ダメージ

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A comprehensive model for plasma process-induced physical damage (ion bombardment damage) on Si substrate surface was proposed. The physical damage is widely regarded as a critical issue for development of aggressively scaled metal–oxide–semiconductor field-effect transistors (MOSFETs) because the damaged layer induces degradation of MOSFET performance. This article focused on “Si recess” in the source / drain extension region – Si loss by a subsequent wet-etching of the layer formed by physical damage. A unified model was presented, describing a quantitative relationship between the energy of incident ion, Si recess depth, and the threshold voltage shift of MOSFET. Based on the analytic models, a framework was proposed for predicting MOSFET degradation induced by the plasma damage.

1. Introduction

Plasma processing plays an important role in manufacturing metal–oxide–semiconductor field–effect transistors (MOSFETs)[1]. Plasma process-induced damage (PID) has been one of the crucial problems for fabricating MOSFETs. PID consists of three major mechanisms, namely, charging damage (PCD), radiation damage, and physical damage (PPD)[2]. PCD is induced by conduction current from plasma flowing into MOSFETs, and commonly referred to as the antenna effect[2]. PPD, on the other, is induced by high-energy ion bombardment on Si substrate or other material surfaces. One of the PPD recently focused on is Si loss in the source and drain extension region, called "Si recess"[3]. Si recess induces the threshold voltage shift ΔV_{th}[4] degrading the MOSFET performance. There have been many reports[3,5,6] discussing the effects of plasma process condition on Si recess formation. However, at present, few models are proposed describing a quantitative relationship between respective plasma and device parameters. In developing future high-performance MOSFETs, a comprehensive PPD model is requisite for optimizing plasma process parameters and designing device structure. In this article, a unified PPD model is presented by clarifying (1) damaged-layer creation, (2) Si recess formation, and (3) MOSFET performance change by PPD.

2. Plasma-induced physical damage

During more than the last two decades, PID has been studied extensively to understand the mechanisms and to solve practical problems with various approaches. Figure 1 illustrates the mechanism of physical damage (surface-damaged layer and defect sites in Si substrate) during an offset spacer etch.

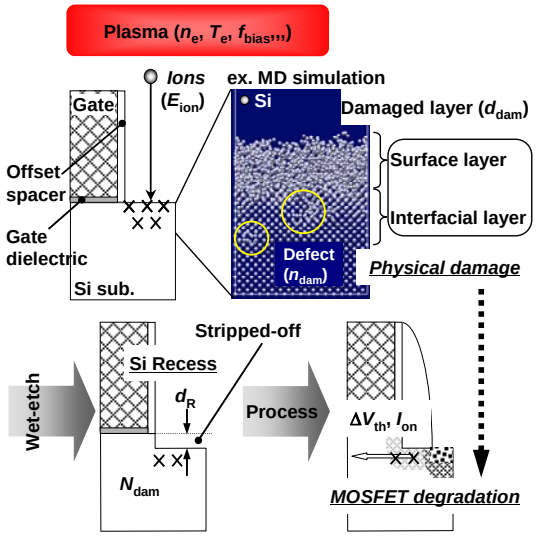

Fig. 1. Damaged-layer and Si recess formation mechanism during an offset spacer etching. This damage leads to MOSFET performance degradation.

There are many factors for PPD mechanism. PPD parameters discussed in this study are defined as follows: The energy of incident ion E_{ion} (obeying the ion energy distribution function IEDF derived from the bias frequency f_{bias}[7]), the damaged layer thickness d_{dam}, the defect site density n_{dam}, the depth of Si recess d_R, the latent areal defect site density N_{dam}, the threshold voltage shift ΔV_{th}, and the drain current (in the linear region) I_{on}. In the next, the relationships among these parameters are provided.

3. A unified PPD model

3.1 *Damaged-layer formation model*

From the modified range theory for PPD[8], n_{dam} at a depth of x is expressed as

$$n_{\mathrm{dam}}(x)dx = \int_{x}^{\infty} \{1+\xi[E_{\mathrm{ion}}(y)]\}\cdot n_{\mathrm{ion}}(y)dy\,, \qquad (1)$$

where n_{ion} and ξ are the projected distribution of ions and the defect generation probability, respectively[8]. d_{dam}, in practice, is defined by conventional monitoring techniques. Although it depends on the resolution of such techniques, one can write for the identified thickness d_{dam} as

$$d_{\mathrm{dam}} = A_{\mathrm{p}}\cdot\left(\overline{E}_{\mathrm{ion}}\right)^{\alpha}, \qquad (2)$$

where A_{p} and α are the process- and material-dependent parameters. $\overline{E}_{\mathrm{ion}}$ is the average ion energy.

3.2 *Si recess formation model*

Since the amount of Si loss depends on the wet-etch time (actually determining d_{R}), d_{R} and N_{dam} are in the trade-off relationship[9] expressed as

$$N_{\mathrm{dam}} = \int_{d_{\mathrm{R}}}^{\infty} n_{\mathrm{dam}}(x)dx\,. \qquad (3)$$

By reviewing various cases, one can write[10]

$$d_{\mathrm{R}} = a\left(\overline{E}_{\mathrm{ion}}\right)^{\beta}, \qquad (4)$$

where a and β are the process- and material-dependent parameters.

3.3 *MOSFET degradation model*

As mentioned above, MOSFETs with PPD suffer from the performance degradation. ΔV_{th} and I_{on} of the damaged MOSFET were modeled[4,11] as

$$\Delta V_{\mathrm{th}} \approx -B\cdot d_{\mathrm{R}}\,, \qquad (5)$$

and

$$I_{\mathrm{on}}^{\mathrm{dam}} = I_{\mathrm{on}}^{0}\cdot\left(1-C\cdot N_{\mathrm{dam}}\right), \qquad (6)$$

where B and C are the device structure-dependent parameters. I_{on}^{0} is the drain current of no-damaged MOSFET.

3.4 *Predicted MOSFET degradation*

By unifying the above models, one can predict MOSFET performance degradation by PPD "directly" from plasma parameters. Figure 2 shows an example of predicted results – ΔV_{th} versus $\overline{E}_{\mathrm{ion}}$ for an Ar-plasma exposure case. (The applied bias frequency was assumed in the low frequency limit where all the ions can respond to the time-varying sheath-voltage drop[7].) As seen, ΔV_{th} exhibits a power-law dependence on $\overline{E}_{\mathrm{ion}}$, regardless of gate lengths. (Note that this power-law is attributed to (4) and (5).) Thus, it is suggested that one can design (estimate) MOSFET performance change by PPD, i.e., one can optimize the device structure and plasma process condition in advance.

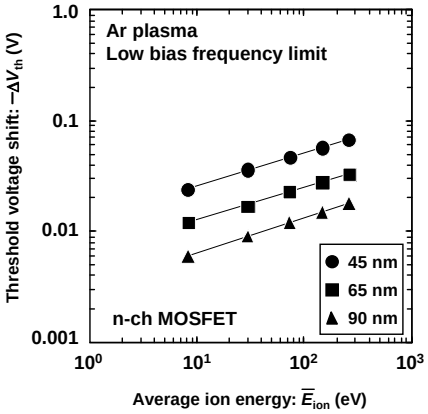

Fig. 2. Predicted ΔV_{th} as a function of the average incident ion energy for various gate lengths (45, 65, and 90 nm).

4. Summary

Plasma process-induced physical damage to MOSFET was modeled. A prediction framework was proposed by using the PPD models. The presented models should be implemented in future scaled microelectronic device design.

Acknowledgments

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