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Numerical Simulation of Plasma-induced Charging during SiO_2 Etching

SiO_2プラズマエッチング中のチャージングシミュレーション

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A series of our works on a charging problem during SiO_2 etching of high-aspect contact hole (HARC) is introduced. A surface conduction, one of possible mechanisms for reducing the excessive charge accumulation at the bottom of the hole exposed to fluorocarbon-based plasma for SiO_2 etching, is investigated by using both an experimental technique and a numerical model. In addition, a gate tunneling current is also combined to the model under the presence of a lower gate electrode. The charging voltage is reasonably coincides with a practical value in industry under the typical condition for HARC plasma etching.

1. General

Top-down plasma processing is increasingly important for a continuous development of ultra large scale integrated (ULSI) circuits. In particular, etching of contact holes through SiO_2 film to Si or silicon nitride layers is a crucial process for the fabrication of multilayer interconnects. In past two decades, dry etching technology of high aspect-ratio contact hole (HARC) has been suffering from a number of difficulties, such as RIE-lag, Si recess, etch stop, and breakdown of gate oxide, with a further shrinkage of design rule to sub-nm. According to ITRS roadmap in 2010, contact hole with the aspect-ratio of more than 20 and the size of a few ten of nanometers is required for DRAM device. A local charge accumulation caused by a charge separation inside the hole, i.e. an electron shading effect, during SiO_2 etching is classified as one of the origin of plasma-induced damages (PID).

Reactive ion etching (RIE) of SiO_2 using fluorocarbon gas chemistry proceeds under the competition of surface protection by the deposition of neutral radicals (C_xF_y) and chemical sputtering by energetic ions. Under a practical condition, etched surface is steadily covered with polymer layer made of CF radicals. At the same time, sidewall is protected against the energetic ions by polymer deposition. Therefore, the polymer film on the sidewall with finite conductivity has big influence on charge accumulation, resulting in the characteristics of SiO_2 etching.

In this study, charging voltage accumulated in the hole is investigated in terms of surface conduction at the sidewall by using experimental and numerical methods in order to estimate the surface conductivity. Then, the charging voltage is also calculated with a gate electrode taking a tunneling current into account.

2. Methodologies

Charging voltage measurement system embedded in a two-frequency capacitively coupled plasma (2f-CCP) chamber is shown in Fig. 1. Two types of chips, a hole-patterned SiO_2 chip and a blanket Si chip, are set on the electrode biased by the low frequency (LF: 500 kHz) source in order to measure the bottom potential of both chips by using a pair of high-voltage probes. A powered electrode driven by very high frequency (VHF: 100 MHz) source is located at the opposite of the LF source. The difference of the bottom potential between two chips was defined as the charging voltage.

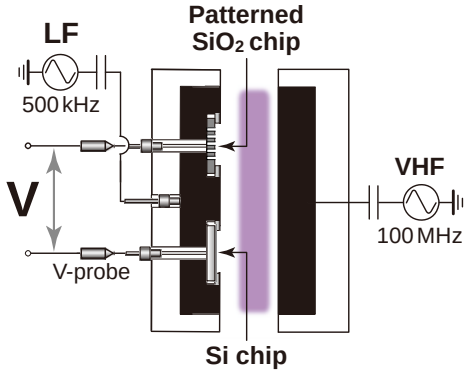

Fig. 1: Schematic of the arrangement of patterned SiO_2 and flat Si chips for measurement of the bottom charging voltage.

Temporal evolution of the local surface potential inside the geometrically fixed structure was traced by a particle simulation with Poisson's equation as a function of aspect-ratio,

$$\nabla^2 V(x,z,t) = \begin{cases} -e\frac{n_p(x,z,t)-n_e(x,z,t)}{\varepsilon_0} & \text{in gas phase} \\ -\frac{\rho_s(x,z,t)}{\varepsilon} & \text{on } SiO_2 \\ 0 & \text{in } SiO_2 \end{cases},$$

where V is the potential, n_p and n_e are the number density of positive ions and electrons, respectively. Two-dimensional (x, z) trench structure with periodic boundary was considered in a SiO_2 layer on a grounded Si substrate. The details of the charging simulation can be referred elsewhere [3].

3. Results and Discussion

The comparison of the charging voltages obtained from the experiment and the simulation is shown in Fig. ○ as a function of voltage amplitude of the biased LF electrode, V_0. In the experimental result (Aspect Ratio = 5), the charging voltage increases almost linearly with V_0, and then saturates to the value of ~ 30 V. On the other hand, the simulated result simply shows a linear increase with increasing V_0, and finally approaches to several hundred of volts. The difference of both charging voltages ΔV can be explained by the surface conduction current on the sidewall as a possible mechanism for relaxing the charge buildup at the bottom of the patterned SiO_2 chip. When the surface conductivity σ was taken to be 1.0 x 10^{-8} $\Omega^{-1}cm^{-1}$, the charging voltage at V_0 = 300 V and AR = 5 reduced to 48 V, as also shown in Fig. 2 (◆). This indicates that the optimal value of the surface conduction current J_e can be determined by comparing the experimental and numerical results by controlling σ as ΔV ~ 0.

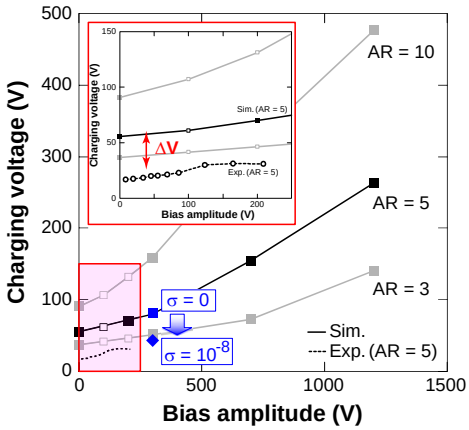

Fig. 2: Charging voltage as functions of voltage amplitude of the biased electrode and aspect ratio of the patterned SiO_2 chip. Dotted line: experimental, solid lines: simulation.

Furthermore, we investigate the influence of the underlying gate structure on the charging voltage V_{ch} by considering the tunneling current flowing through a thin gate oxide (~ nm). Gate oxide voltage V_{ox} gives the complex behavior as shown in Fig. 3. When the etching proceeds and the aspect-ratio of the hole increases, V_{ch} linearly increases and V_{ox} keeps almost constant. On the other hand, under the condition of aspect-ratio > 7, V_{ch} drastically decreases and V_{ox} gradually increases due to the contribution of the tunneling current.

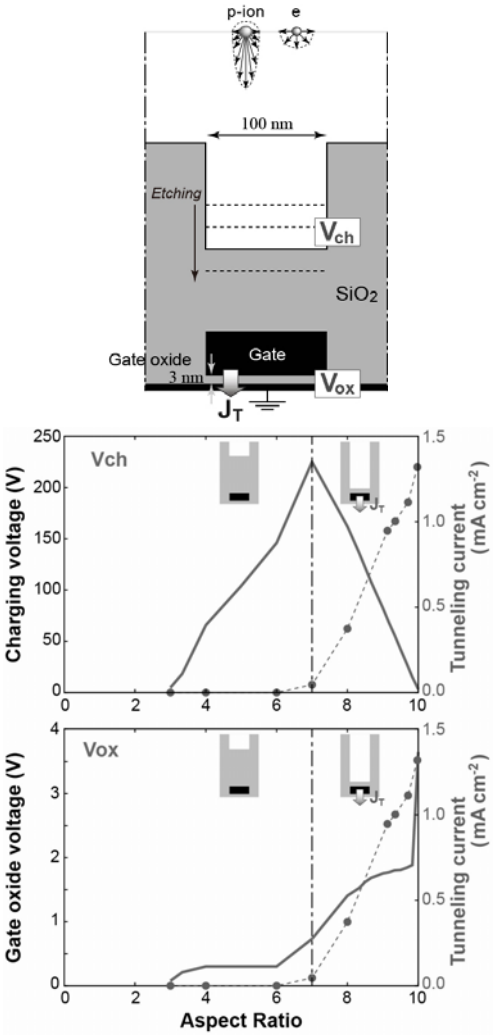

Fig. 3: Charging voltage at the bottom of the hole V_{ch} and gate oxide voltage V_{ox} as a function of aspect-ratio (right side).

Acknowledgments

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References

[1] T. Ohmori and T. Makabe: Appl. Surf. Sci. **254** (2008) 3696.

[2] J. Matsui, T. Makabe, et al: J. Phy. D **34** (2001) 2950.

[3] T. Yagisawa et al., Proc. 63rd GEC, (2010).