Improvement of Electrical Device Performances for Graphene Directly Grown on a SiO_2 Substrate by Plasma Chemical Vapor Deposition

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The electrical device performances of graphene directly grown on a SiO_2 substrate have been improved through the precise adjustment of growth conditions such as growth temperature and growth time in plasma chemical vapor deposition (CVD). Only at the suitable combination of growth time and temperature, high quality and uniform graphene sheet can be directly grown on a SiO_2 substrate. Forward and reverse sweeps of source-drain current (I_{ds}) vs. gate bias voltage (V_{gs}) showed small hysteresis, possibly caused by the clean surface of the graphene device fabricated by plasma CVD, a technique that did not involve any transfer. Four-point probe measurements to evaluate the intrinsic sheet resistance of the fabricated graphene showed its value to be 170 - 200 Ω/sq, a value much lower than that of graphene directly grown on SiO_2 substrate by other techniques. This low sheet resistance possibly originated from the high quality of graphene obtained by plasma CVD. These observations suggest that graphene directly grown on SiO_2 substrate by plasma CVD should be a very promising candidate for fabrication of graphene-based high-performance electrical devices.

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Graphene is monolayered carbon sheet with excellent properties such as high carrier mobility, high transparency, and high mechanical flexibility, which make it a promising candidate for future applications to flexible high-performance electrical devices [1, 2]. Generally, graphene is grown on the surface of a metallic foil by chemical vapor deposition (CVD) [3, 4], and, for the fabrication of graphene-based electrical devices, this graphene is transferred to an insulating substrate such as a SiO_2 [5, 6]. During this transfer, a lot of defects and impurities are introduced into graphene, which results in poor device performance. Direct growth of graphene on an insulating substrate is another approach for the fabrication of graphene-based electrical devices, and various investigations in this regard have been carried across the world [7–10]. Since the direct growth of graphene on an insulating substrate does not require any transfer process, better performance of the graphene-based device can be expected as compared with that of the graphene-based device fabricated via the transfer process. Recently, we realized the direct growth of graphene on SiO_2 substrate by plasma CVD [10]. Plasma CVD is known as a powerful method for low temperature and large area growth of nanocarbon materials compared with thermal CVD. However, the sheet resistance of graphene growth by our previous method was moderate (~2000 Ω/sq) compared with other graphene directly grown on an insulating substrate by thermal CVD, and further progress is necessary for future fabrication of graphene-based high-performance electrical devices.

In this communication, we report the improvement of electrical device performances of graphene directly grown on a SiO_2 substrate through the adjustment of growth process in plasma CVD. Four-point probe measurements with Hall-bar structures were employed for the estimation of intrinsic electrical performance of the graphene. Based on these detailed measurements, it was found that the graphene device showed very small hysteresis in the plots of source-drain current (I_{ds})-gate bias voltage (V_{gs}). Furthermore, the sheet resistance of graphene directly grown on the SiO_2 substrate showed a low value (170 - 200 Ω/sq). These observations are possibly the result of the clear surface and the high quality of the transfer-free graphene device.

Graphene growth was carried out by a homemade plasma CVD reactor, and a mixture of CH_4 and H_2 gases was used; detailed explanations of the procedure and equipment used can be found elsewhere [10]. Graphene structure was evaluated by Raman scattering spectroscopy with He-Ne laser (Horiba HR-640) excitation at 632.8 nm wavelength. Electrical performance of graphene and its intrinsic sheet resistance were measured by a four-point probe method using a vacuum probe station (Nagase GRAIL 10-101-4-LV-HT) and a semiconductor parameter analyzer (Agilent 4155C). The advantage of employing

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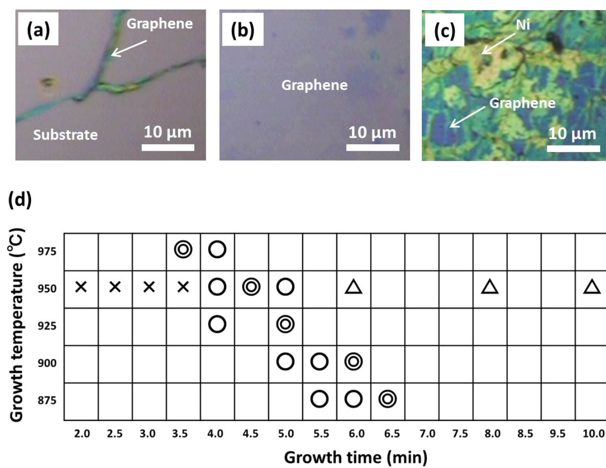

Fig. 1 Typical optical microscope images of the substrate after plasma CVD with different growth time of (a) 2.5 min, (b) 4.5 min, and (c) 10 min at 950°C followed by Ni etching. (d) Correlation of growth temperature and growth time for the morphology of graphene. The symbol of ◎, ○, △, and × in (d) denotes that graphene growth as uniform sheet (b), partial sheet, sheet with Ni residue (c), and fiber-like curly structure (a), respectively.

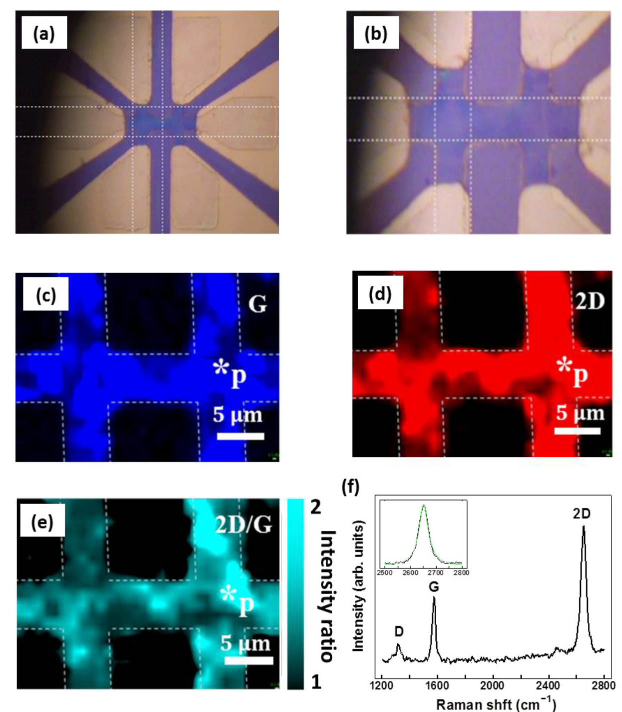

Fig. 2 (a) Low- and (b) high-magnification optical microscopy images of graphene device with Hall-bar structures. (c-e) Mapping images of Raman scattering spectra of graphene, exhibiting the (c) G-peak, (d) 2D-peak, and (e) ratio of the 2D to G peak intensities. (f) Typical raw Raman scattering spectra of graphene taken at the position "*p*" shown in (c-e). Inset in (f) shows a fitting curve of 2D-peak using single Lorentzian function.

such a method is that the adverse effects of contact resistance between electrode and probe are nullified [11].

The detailed adjustment of growth time and growth temperature was carried out to improve the quality of graphene. Figures 1 (a-c) show typical optical microscope images of substrate after plasma CVD followed by Ni etching. When growth time is short, small peace of graphene can be obtained with curled shape, which should be formed during the etching process of Ni (Fig. 1a). Longer growth time results in growth of graphene both under and top of Ni (Fig. 1c). The Ni covered by graphene can not be removed even with long time HCl etching. Only with the suitable growth time, uniform graphene sheet can be obtained as shown in Fig. 1b. This optimum growth time has a clear temperature dependence and becomes short with an increase in the growth temperature (Fig. 1e). This should be due to the difference of diffusion coefficient of carbon in Ni. Based on this result, it was found that high temperature (950°C) with relatively short growth time (~4.5 min) can realize the direct growth of graphene with relatively high quality and uniform sheet structures. Figure 2 shows optical microscopy (Figs. 2 (a), (b)) and Raman mapping (Figs. 2 (c)-(e)) images of graphene grown directly on a SiO_2 substrate by plasma CVD under the optimum growth condition. Mapping images of Raman scattering spectra of G-peak, 2D-peak, and ratio of the 2D to G peak intensities are shown in Fig. 2 (c), Fig. 2 (d), and Fig. 2 (e), respectively. Hall-bar structures of Ni were pre-deposited on the SiO_2 substrate, which was patterned using a photolithography technique. Then, plasma CVD was carried out, followed by conventional Ni etching with an HCl solution. Since graphene can be grown along the interlayer between Ni and SiO_2 by our method [10], the Hall-bar structures of graphene can be directly formed on the SiO_2 substrate without any transfer process. Hall-bar structures of electrodes were formed on the top of the graphene layer using a photolithography technique. Clear G and 2D peaks, observed in the Raman mapping images (Figs. 2 (c)-(e)), were only from the area where Ni catalysts were pre-deposited. As can be seen, 2D peak intensities are higher than G peak intensities. The 2D peaks, fitted using single Lorentzian function (inset in Fig. 2 (f)). Intensities of D peak, relating with the impurity and defect in graphene, are much lower than G peak intensities. These observations indicate that the graphene directly grown on the SiO_2 substrate is either a monolayer or a few layers thick and is of high quality. Small variations in the intensity ratios of 2D to G peaks appear, however, depending on the position on the graphene, possibly caused not by the layer number ununiformity of graphene but by the differences in the degree of interaction with the substrate.

Electrical device performances were measured under high-vacuum condition at room temperature as shown in Fig. 3 (a). The I_{ds}-V_{gs} curves show enhanced p-type electrical transport properties, with I_{ds} monotonically decreas-

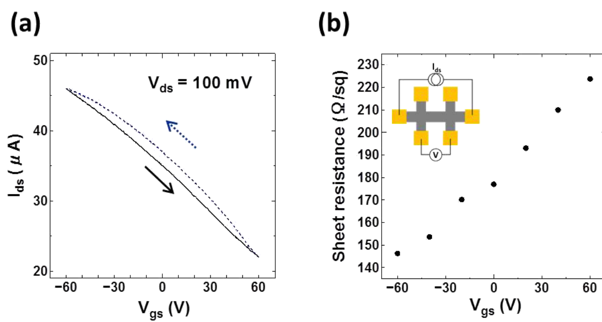

Fig. 3 (a) Typical I_{ds}-V_{gs} curve of graphene (V_{ds} = 100 mV). (b) V_{gs} dependence on sheet resistance of graphene, measured by four point probe measurement. Inset in (b) shows a schematic illustration of the four-point probe measurement.

ing with increasing V_{gs}. This is because of the hole doping of graphene from the SiO_2 substrate due to the naturally strong interaction tendencies between graphene and SiO_2. This strong doping of graphene directly grown on SiO_2 is consistent with the results stated in our previous report [10] and those reported by another group [7]. Forward and reverse I_{ds}-V_{gs} curves are shown in Fig. 3 (a). Both forward and reverse sweeps show almost similar curves with very small hysteresis, because of the clean surface of the graphene fabricated by the transfer-free process. This low hysteresis is very important for the future fabrication of graphene-based high performance electrical devices. Based four-point probe measurements, sheet resistance of the fabricated graphene was found to be about 170 - 200 Ω/sq (Fig. 3 (b)), a value much lower than that of graphene directly grown on SiO_2 substrate by thermal CVD (~2000 Ω/sq) [7–9]. It was revealed that the hexagonal domain graphene with relatively large domain size (> 10 μm) was directly grown on the SiO_2 substrate by our method [10]. The hexagonal domain graphene with large domain size is known as a single crystal of graphene with high quality, which can suppress the negative effects in electrical transport such as a grain boundary scattering of electrical carriers. Since the growth of hexagonal domain graphene is possible only by the indirect growth with thermal CVD on Cu surface except for our method, graphene directly grown on the SiO_2 substrate by other method show relatively high sheet resistance. It can be conjectured that the grain size of graphene increased through the precise adjustment of growth conditions, resulting in the low sheet resistance. The detailed effects of plasma on the direct growth of high quality graphene are under investigations.

In summary, we have realized the improvement of electrical device performances for graphene directly grown on a SiO_2 substrate through the precise adjustment of growth process in plasma CVD. Forward and reverse sweeps of I_{ds}-V_{gs} curves show very low hysteresis. Four-point probe measurements show that the intrinsic sheet resistance of the obtained graphene is 170 - 200 Ω/sq, a value much lower than that of graphene grown directly grown on SiO_2 substrate by thermal CVD. Such directly grown graphene, with its advantages of small hysteresis and low sheet resistance, is expected to be very useful for the future fabrication of high-performance graphene-based electrical devices.

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