Temporal Analysis of Electrostatic Chuck Characteristics in Inductively Coupled Plasma

Gyu Il SHIM and Hideo SUGAI[1)]

Department of Electrical Engineering and Computer Science, Nagoya University, Nagoya 464-8603, Japan
[1)]Department of Electronics and Information Engineering, Chubu University, Kasugai 487-8501, Japan

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Johnsen-Rahbek electrostatic chuck (ESC) for holding a silicon wafer in semiconductor processing is investigated in inductively coupled plasma (ICP). Bi-layer model of the ESC consisting of a thick bulk layer and a thin interface layer is proposed. The resistance of each layer is obtained by measuring the ESC voltage-current (V-I) characteristic with and without the wafer in ICP, along with the voltage effectively applied to the interface layer. Surface charges stored in the interface layer capacitance are found by the time-integration of current in a turn-on phase of a ramped voltage. On the other hand, the chuck holding force is *in situ* obtained in a turn-off phase of slowly ramped voltage, from the critical conditions of helium gas pressurization for wafer de-chuck. The electrostatic force predicted on a basis of equivalent circuit in the bi-layer model coincides with the mechanical force obtained in the wafer de-touch experiments.

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In plasma-assisted processing of semiconductors, electrostatic chuck (ESC) has been widely used for holding a silicon wafer on stage in vacuum. Two types of ESC are used; Coulomb type [1–3] using insulating spacer layer (volume resistivity $\rho > 10^{14}\,\Omega$-cm), and Johnsen-Rahbek type [4, 5] using semiconductive spacer layer ($\rho = 10^{10}$-$10^{12}\,\Omega$-cm) between the plates (i.e., chuck electrode and wafer). The electrostatic holding force stems from the opposite polarity surface charges appearing on the wafer and the chuck electrode at high applied voltages. In the J-R type, very strong holding force is achieved at lower chuck voltages than in the Coulomb type, owing to the high electric fields between the narrow gaps distributed over the spacer layer with surface irregularities. However, the J-R type is complex and sensitive to various interface parameters such as electrical conductivities, surface roughness on sub-microscopic scale, and large-scale flatness of two plates. And the ESC often leads to troubles such as poor process repeatability caused by residual charges, film damages induced by the chuck current, and wafer crack during lift by pins for wafer replacement.

To avoid such troubles, a deeper understanding of the J-R type ESC is required, particularly in practical plasma conditions. In a previous paper [6], we reported remarkable effects of RF-induced self-bias voltage on the ESC voltage-current (V-I) characteristics which was observed in low-density capacitively-coupled plasma (CCP). In this paper, we present temporal analysis of J-R type ESC characteristics in high-density inductively-coupled plasma (ICP). The time-integration of chuck current during a voltage turn-on phase gives surface charges at the interface while the turn-off phase variation of pressurized helium flow behind a wafer enables evaluation of the electrostatic holding force. Bi-layer equivalent circuit model is proposed to explain the behavior of the J-R type ESC.

The experiment was performed in an ICP device [7] where plasma is produced in a cylindrical stainless steel chamber, by 13.56 MHz RF discharge in argon at a typical pressure of 0.1 Torr. A 200-mm-diam J-R type electrostatic chuck is installed in the apparatus. The chuck electrode made of molybdenum is embedded in a 5 mm thick aluminum nitride (AlN) with separation $l = 0.54$ mm (spacer layer thickness) from the contacting wafer surface. The geometrical contact area of ESC is 60 % of the projected area of chuck electrode, owing to a number of emboss (height 50 μm, area 2×2 mm^2) prepared for helium gas cooling of wafer.

First of all, the chuck current I_0 flowing from the chuck electrode via a 200-mm-diam silicon wafer to the grounded chamber wall was measured as a function of the chuck voltage V_0 from -1 kV to $+1$ kV in 600 W discharge at argon 0.1 Torr. As indicated by open circles and crosses in Fig. 1, the chuck current $|I_0|$ was observed to be slightly larger for the negative chuck voltage than for the positive voltage at the same absolute value of $|V_0|$. This phenomenon is explained in terms of self-bias effect [6]: the floating wafer has the surface potential $V_W \sim 12$ V in the present ICP discharge, and hence the magnitude of effective voltage ($V_{\text{eff}} = V_0 - V_W$) applied between the chuck

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author's e-mail: sugai-h@isc.chubu.ac.jp

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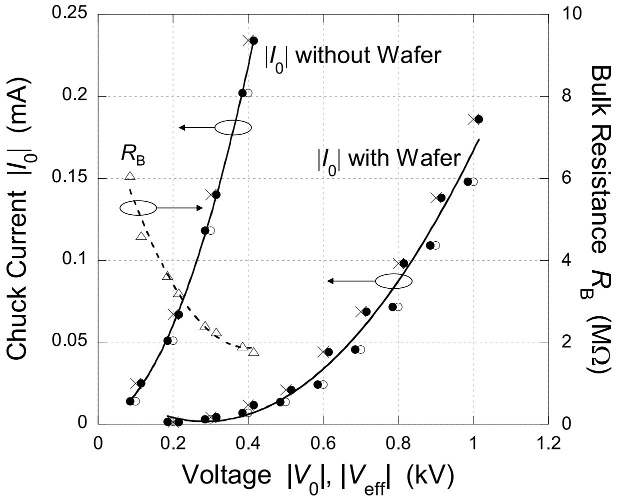

Fig. 1 Chuck current I_0 vs. chuck voltage $|V_0|$ with and without wafer measured in ICP, along with bulk resistance $R_B = |V_{eff}|/|I_0|$ obtained without wafer. Open circle and cross indicate the data for $V_0 > 0$ and $V_0 < 0$, respectively. Closed circle and solid line indicate the values corrected for the effective voltage $V_{eff} = V_0 - V_W$.

electrode and the wafer is larger for negative V_0. The closed circles in Fig. 1 indicate the current plotted against the effective voltage. The ratio of $|V_{eff}|$ to $|I_0|$ in Fig. 1 gives the total resistance R_T consisting of contact resistance and bulk resistance R_B of AlN layer. The values of R_T are ~ 40 MΩ at $|V_0| = 0.4$ kV, ~10 MΩ at 0.7 kV, and ~6 MΩ at 1 kV. However, these values are much larger than the resistance of AlN spacer layer $R_B \sim 3$ MΩ which is estimated assuming $\rho \sim 2 \times 10^{10}$ Ω-cm after the Ohm's law for the 200-mm-diameter 0.54-mm-thick AlN layer.

Such very high resistances observed at low chuck voltages clearly suggest an existence of high contact resistance at the interface between the wafer and the chuck surface. In order to find the bulk resistance eliminating the contact resistance, we exposed the chuck surface directly to plasma (600 W, 0.1 Torr) without wafer and measured the chuck current as shown in Fig. 1. Much better contact of the chuck and plasma allows high currents at low voltages. The bulk resistance $R_B = |V_{eff}|/|I_0|$ plotted by triangles is as low as ~2 MΩ at $V_0 > 0.2$ kV. The resistance at lower voltages gradually increases, probably due to an increase in the contact resistance still remaining even in case of plasma exposure of ESC.

Based on the measurements in Fig. 1, we propose bilayer model of the J-R type ESC as illustrated in Fig. 2 (a), along with an equivalent circuit in Fig. 2 (b). Here the AlN spacer layer between the chuck electrode and the silicon wafer is divided into two layers: one is a thick ($l = 0.54$ mm) bulk layer of resistance R_B, and the other is a thin interface layer of thickness δ expressed by a resistance R_I and a vacuum capacitance C_I where $C_I = \varepsilon_0 S_I/\delta$ assuming the net area S_I. It is notable in this model that a bulk layer capacitance is negligible compared with the interface layer capacitance C_I because of $\delta << l$. The total resistance discussed above is given by $R_T = R_B + R_I$. The V-I characteristic in the presence of wafer in Fig. 1 manifests a strongly nonlinear variation of the interface resistance R_I with respect to the voltage V_{eff}. Such nonlinearity is one of the evidences of Johnsen-Rahbek effect [8] and is attributed to field emission of electrons [9, 10] under intense electric field as reported previously [7]. A relatively uniform current passing through the bulk layer is squeezed into numerous uneven contact points of the interface layer surface, which in turn leaves the surface charge Q_0 around contact points. The opposite polarity charges on the wafer and the chuck form the distributed vacuum capacitances with an average gap of δ, causing the electrostatic holding force. These charges are continuously lost and supplied by the DC chuck current I_0 flowing through the surface resistance R_I. Thus, the following two relations stand in the bi-layer model:

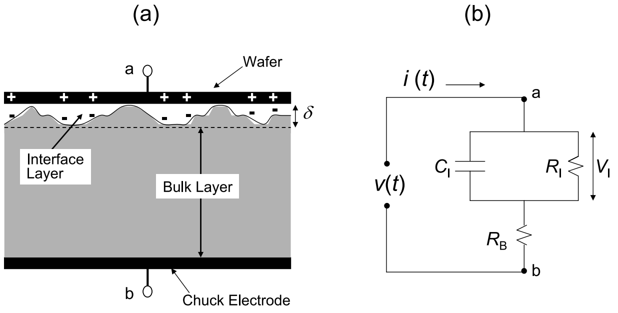

Fig. 2 (a) Bi-layer model of J-R type ESC and (b) equivalent circuit.

$$V_I = R_I I_0, \quad Q_0 = C_I V_I. \tag{1}$$

In order to find the chuck charge Q_0 in steady state, we applied a ramped voltage and measured a charging current of square-wave form as shown in Fig. 3 (a) where the voltage linearly increases in time to a top value $V_0 = 0.8$ kV with the ramp time $\tau_R \sim 1$ ms. Although the results are not shown here, the discharging current of the same magnitude flows in the opposite direction during the voltage turn-off phase. In Fig. 3 (a), a large charging current of ~13 mA is observed for -0.4 ms $< t < 0.4$ ms during the turn-on phase, and subsequently for t > 0.4 ms a small DC current ($I_0 \sim 0.08$ mA measured by DC ammeter) flows where spiky currents visible in Fig. 3 (a) are spurious signals induced by circuit regulation. The time integration of chuck current $i(t)$ for the ramp time τ_R gives the chuck surface charge Q_0. According to this technique, the charge stored on the wafer interface was measured for various chuck voltage V_0 (< 0) in the 600 W discharge. Here we define the interfacial voltage $V_I = V_{eff} - R_B I_0$ which is the voltage applied to the interface layer (C_I and R_I) as noted in Fig. 2 (b). The charge $|Q_0|$ measured as a func-

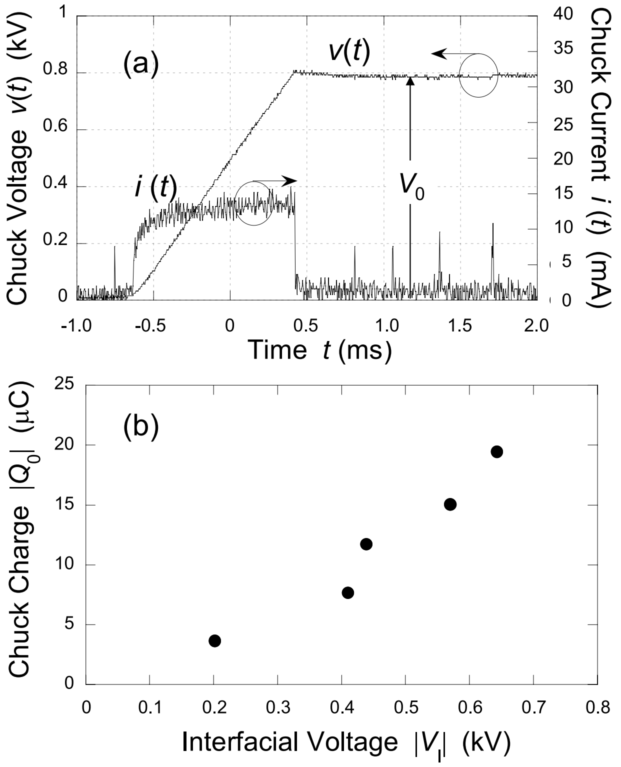

Fig. 3 (a) Time variations of ramped chuck voltage $v(t)$ and current $i(t)$, (b) chuck charge $|Q_0|$ as a function of interfacial voltage $|V_\mathrm{I}|$ in ICP at 600 W and 0.1 Torr.

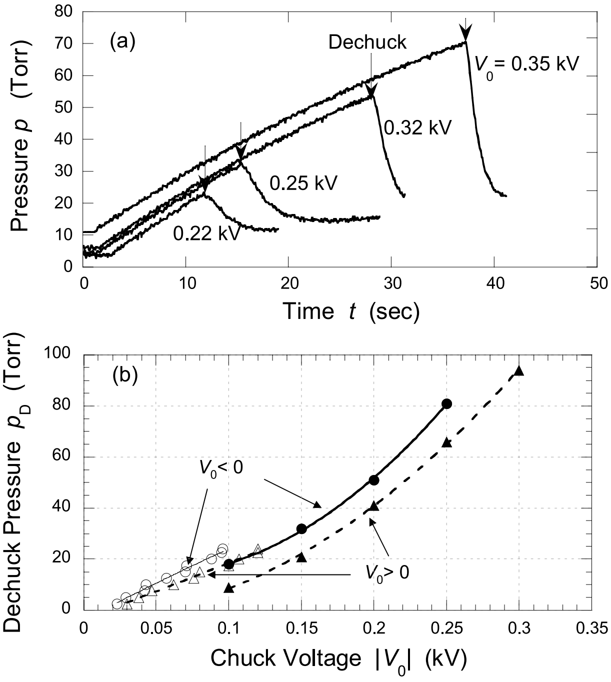

Fig. 4 (a) Time evolution of helium pressure for different chuck voltages at 10 sccm helium injection, and (b) de-chuck pressure vs. chuck voltage for negative V_0 (circles) and positive V_0 (triangles) measured in constant flow mode (closed symbols) and constant pressure mode (open symbols) in ICP at 1000 W and 0.1 Torr.

tion of the interfacial voltage $|V_\mathrm{I}|$ is shown in Fig. 3 (b). In contrast to conventional capacitances, the charge is not linearly proportional to the applied voltage. Using the measured Q_0, we can obtain the interfacial layer capacitance $C_\mathrm{I} = |Q_0|/|V_\mathrm{I}|$ from Eq. (1), which increases from 18 nF at 0.2 kV to 30 nF at 0.64 kV. Such an increase in the capacitance with the voltage is tentatively attributed to a decrease in the gap distance δ due to compression by the stronger electrostatic holding at higher voltages.

The surface roughness of silicon wafer measured by AFM (Atomic Force Microscope) is 0.8 ~ 1.6 μm. Keeping this value in mind, we assume the overall average gap distance to be $\delta \sim 5\,\mu\mathrm{m}$ at the low voltage of 0.2 kV, considering the roughness and the flatness of two surfaces (the chuck surface and the wafer surface). Then, the measured capacitance of 18 nF at 0.2 kV gives the net area $S_\mathrm{I} \sim 1.02 \times 10^{-2}\,\mathrm{m}^2$. On the other hand, a number of emboss reduce the geometrical contact area of the 200-mm-diam wafer by 60 %, and hence the apparent contact area is $S_* = 1.88 \times 10^{-2}\,\mathrm{m}^2$.

In order to evaluate the electrostatic holding force, we pressurize helium cooling gas flowing in the narrow space of the wafer-chuck interface. When the upward pressure force exceeds the downward ESC force, the wafer is lifted up de-touching from the chuck surface, which induces the temporal changes in the helium pressure and/or flow rate. We made two modes of measurements: one is *constant flow mode*, and the other is *constant pressure mode*.

An example of the constant flow mode is shown in Fig. 4 (a) where helium gas is injected at a constant flow rate of 10 sccm for the given chuck voltages (V_0 = 0.22 kV, 0.25 kV, 0.32 kV and 0.35 kV) in 1000 W discharge. The helium pressure gradually increases in time and drops abruptly at the moment of de-chuck due to considerable gas leakage from the ESC to the plasma chamber. Thus, the highest pressure, i.e., de-chuck pressure p_D observed in Fig. 4 (a) corresponds to the pressure balance with the holding force. The solid dots and triangles in Fig. 4 (b) show the de-chuck pressure dependence on the negative chuck voltage and the positive chuck voltage, respectively. One can see in this figure that the de-chuck pressure is higher for negative V_0 than for positive V_0. The solid and dashed lines indicate the best fit curves for negative and positive, respectively, and the difference between them is ~25 V which coincides with twice the wafer surface potential V_W as discussed above on the data shown in Fig. 1.

In a series of de-chuck experiments, hysteresis phenomena were often observed where the data are significantly influenced by the past experiments. Once the de-chuck takes place, the charges partly remain on the chuck surface, disturbing the subsequent experiments. In order to keep a reproducibility, the wafer after de-chuck was transferred to a load-lock chamber, and the chuck surface was

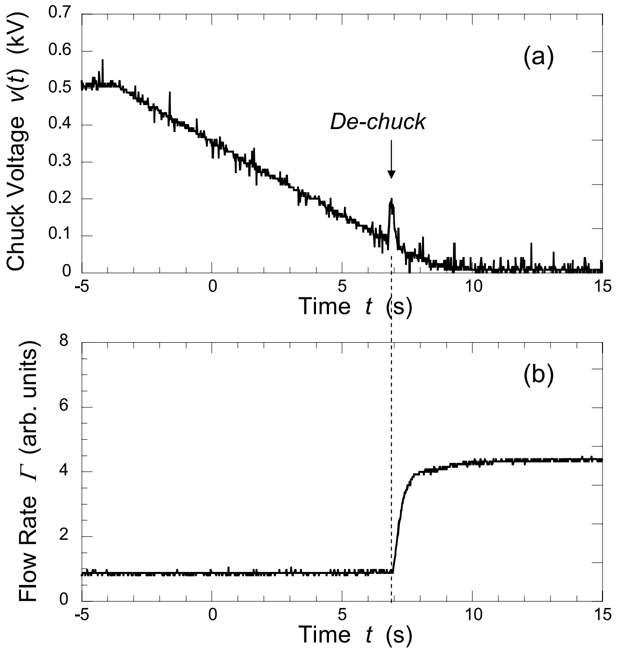

Fig. 5 Time evolution of (a) ramped chuck voltage $v(t)$ and (b) helium flow rate Γ in ICP at 1000 W and 0.1 Torr.

exposed to argon plasma in 0.1 Torr argon for 30 seconds to remove the residual charges on the chuck. This charge removal process was inevitable for reliable data acquisition.

An accuracy of the *constant flow mode* measurement is degraded for $|V_0| < 0.15$ kV due to small signals with blunt variation. Thus, in the low-voltage range, we employ a more precise technique of *constant pressure mode* with slowly ramped chuck voltage v(t), as demonstrated in Fig. 5. The chuck voltage of $V_0 = 0.5$ kV starts to decrease at $t = -3.5$ s with a sufficiently slow decay rate of ~10 s while the helium pressure is kept constant at $p = 10$ Torr by feedback control of the flow rate. As seen in Fig. 5 (b), the flow rate abruptly increases at $t = 7$ s when the wafer is de-touched from the chuck surface at 0.07 kV. After de-touching, the flow rate reaches the maximum value (50 sccm) of the present mass flow controller. It should be noted in Fig. 5 (a) that a sharp spiky signal appears in the chuck voltage just at the de-chuck moment ($t = 7$ s) due to impedance change.

When the helium pressure is set to be higher than 10 Torr, the de-chuck occurs at the time earlier than 7 s, corresponding to the higher de-chuck voltage. In this way, the constant pressure mode enables precise determination of the de-chuck pressure as function of the chuck voltage. The data measured below 23 Pa are plotted, in Fig. 4 (b), by open circles and triangles for the negative and positive V_0, respectively. At $|V_0| = 0.1$ kV, this accurate method gives about two times larger de-chuck pressure ($p_{\mathrm{D}} \sim 20$ Torr) compared with the data obtained at the constant helium flow rate.

The pressurized helium gas pushes the wafer area $S_{\mathrm{M}} = 1.26 \times 10^{-2}\,\mathrm{m}^2$ (40 % of the 200-mm-diam wafer) except for the net area S_{I}. Thus, the mechanical force by helium gas compression at the de-chuck point is given by

$$F_{\mathrm{M}} = p_D S_{\mathrm{M}}. \tag{2}$$

On the other hand, the electrostatic force F_{E} provided by the surface charge Q_0 in a vacuum condenser is given by

$$F_{\mathrm{E}} = (D^2/2\varepsilon_0) S_{\mathrm{I}}, \tag{3}$$

where the electric displacement $D = Q_0/S_{\mathrm{I}}$. At the chuck voltage $|V_0| = 0.1$ kV, the accurate measurement in the constant pressure mode provides $p_{\mathrm{D}} \sim 20$ Torr, which gives the mechanical force $F_{\mathrm{M}} \sim 33.5$ N. On the other hand, the measured charge $Q_0 \sim 2.5\,\mu$C at $|V_0| = 0.1$ kV gives the electrostatic force $F_{\mathrm{E}} \sim 35.3$ N, and hence the two independent measurements coincides each other within the experimental error, supporting the de-chuck condition of $F_{\mathrm{M}} = F_{\mathrm{E}}$.

In conclusion, the fundamental characteristics of Johnsen-Rahbek type ESC installed in ICP apparatus were investigated. Bi-layer model of the ESC consisting of a thick resistive layer and a thin capacitive layer was proposed. Measurements of V-I curves with and without wafer revealed the resistance of each layer. Charging current measurements in the turn-on phase of a ramped voltage provide a new mean of chuck charge monitoring. Such monitoring eventually gives the ESC holding force since the electrostatic force is proportional to the square of surface charge. A precise technique for *in situ* measuring the holding force based on helium gas pressurization in constant pressure mode was developed. The mechanical force determined by this technique agrees with the electrostatic force given by the equivalent circuit model.

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