# Evolution of Ultra-High-Speed CCD Imagers

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This paper reviews the high-speed video cameras developed by the authors. A video camera operating at 4,500 frames per second (fps) was developed in 1991. The partial and parallel readout scheme combined with fully digital memory with overwriting function enabled the world fastest imaging at the time. The basic configuration of the camera later became a de facto standard of high-speed video cameras. A video camera mounting an innovative image sensor achieved 1,000,000 fps in 2001. *In-situ* storage with more than 100 CCD memory elements is installed in each pixel of the sensor, which is capable of recording image signals in all pixels in parallel. Therefore, the sensor was named ISIS, the *in-situ* storage image sensor. The ultimate parallel recording operation promises the theoretical maximum frame rate. A sequence of more than one hundred consecutive images reproduces a smoothly moving image at 10 fps for more than 10 seconds. Currently, an image sensor with ultra-high sensitivity is being developed in addition to the ultra-high frame rate, named PC-ISIS, the photon-counting ISIS, for microscopic biological observation. Some other technologies supporting the ultra-high-speed imaging developed are also presented.

Keywords: high speed, high sensitivity, imager, video camera, ISIS, image sensor

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## 1. Introduction

Since the early 1990's, the authors have been engaged in development of high-speed video cameras. This paper reviews the evolution process of the high-speed video cameras in Kinki University with the outlook for the future.

In 1991, a video camera of 4,500 frames per second (fps) was developed (Etoh, 1992) [1]. The camera had sixteen parallel readout ports and was capable of reading out a part of the full frame. The partial and parallel readout scheme enabled imaging at the world fastest frame rate. The camera is equipped with fully digital memory with no mechanical elements such as a video tape recorder. As the number of recordable consecutive frames was limited by capacity of the digital memory, overwriting function was installed to record the image sequence of the target event within the frame memory by continuously replacing old image signals with the latest ones. The image sensor was designed to fit an MCP-type image intensifier commercialized at the time to fully utilize scarce incident light during the shortened frame interval for the increased frame rate.

The camera was later released to market as PHOTRON FASTCAM and KODAK EKTAPRO HS4540, and became a de facto standard of high-speed video cameras.

In 2001, the authors developed a video camera with the maximum frame rate of 1,000,000 fps (Etoh *et al.*, 2002) [2]. The major innovation was development of a special CCD image sensor for the ultra-high-speed continuous image capturing. Each of the pixels of the sensor is equipped with a linear CCD storage area. The continuously captured image signals are simultaneously stored in the CCD storage attached to each pixel. The simultaneous recording at all pixels allowed recording at the ultra-high frame rate. Therefore, the special CCD image sensor was named "ISIS", the In-situ Storage Image Sensor. At the end of each linear in-situ CCD storage channel, a drain is installed for continuous overwriting recording, which facilitates synchronization of image capturing with occurrence of the target event.

Through applications of the video camera mounting the ISIS to microscopy and transmission electron microscopy, it turned out that the sensitivity of the camera is far below the level required for the ultra-high-speed microscopic imaging. In 2003, a project named "Development of the ultra-high-speed bionanoscope" was set up [3], which makes the ultra-high-speed microscopic imaging possible. The most important component is the PC-ISIS, the photon-counting ISIS with ultra-high sensitivity as well as ultra-high frame rate.

Device simulations of the PC-ISIS revealed that the theoretical maximum frame rate of the sensor is about 100 Mfps with some decrease of dynamic range. Recently, basic research on the PC-ISIS aiming at the frame rate of 100 Mfps in the future has started.

For ultra-high-speed observation, it is impossible to

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overcome difficulty due to the insufficient light intensity only by improvement of the image sensor. Every part of the total system, such as the image sensor, the optics, the illumination subsystem, the timing control system, etc., should be improved and adjusted to maximize efficiency of the system for the very weak light condition.

The pixel size of the ISIS is large with the memory in it, and, thus, the pixel count is not large. Therefore, we are developing technologies to make large-area image sensors. This paper also presents some of the technologies.

## 2. ISIS: Ultra-High-Speed Image Sensor

### 2.1 Structure

The ISIS structure invented by Etoh and Mutoh (2005) [4] is shown in Fig. 1.

The pixel of the ISIS has a large photodiode. One pixel element of the ISIS is composed of the photodiode, an in-situ CCD storage channel stretching downward from the photodiode, and a drain attached at the end of each CCD storage channel. The center of a pixel is at the center of the photodiode, consisting of a pixel grid, which is slightly slanted to the CCD grid. Thus, the chip is mounted in a package in a slanted position as shown in Fig. 2.

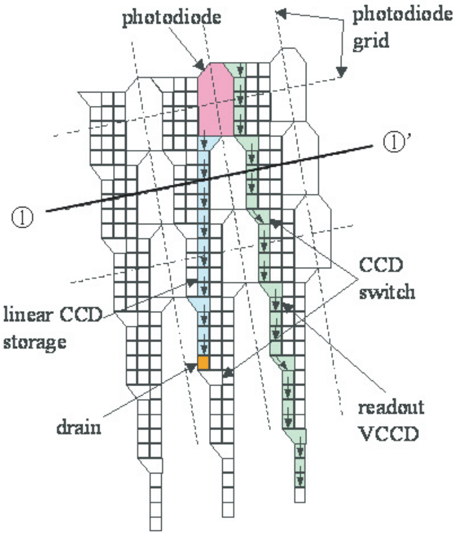


Fig. 1 The basic structure of an ISIS.

Fig. 2 A photograph of a packaged ISIS. The chip is packaged with rotation of a small angle to compensate the slanted configuration of the photodiode/pixel grid shown in Fig. 1.

The storage area is composed of the CCD storage channels and vertical readout CCD channels with short bends stretching beside each column of the photodiodes. A vertical readout CCD consists of a string of the last segments of the in-situ CCD storage elements connected with CCD switches.

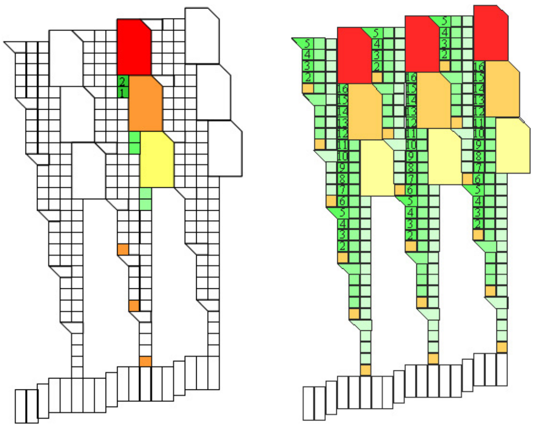
### 2.2 Operations

#### 2.2.1 Image capturing operation

The image capturing operation is shown in Fig. 3. Fig. 3(a) and Fig. 3(b) show the states in which the image signals of the first two frames and of the second to the sixteenth frames are recorded, respectively. In Fig. 3(b), the image signals for the first frame have already been drained to the outside of the sensor through the drain. The image capturing operation with the overwriting continues until the target event occurs and a trigger signal to stop the image capturing operation is released to the sensor.

#### 2.2.2 Readout operation

After the image capturing operation ceased, the image signals stored in the in-situ storage are read out to a buffer memory outside the sensor and, finally, reconstructed as consecutive image frames. At first, the image signals stored in the vertical readout CCDs, i.e., the last segments of the storage CCD elements, are readout through the horizontal readout CCDs. When the vertical readout CCDs become empty, the image signals stored in the storage CCD elements are transferred to the vertical readout CCDs until they are filled with the image signals. The operation is repeated until all the image signals are read out of the sensor



(a) (b)

Fig. 3 Image capturing operation of the ISIS.

and the in-situ storage CCDs become empty.

## 2.3 Test sensor and example image

The first sensor of the ISIS was developed in 2001, named ISIS-V2, and mounted on a camera developed by Shimadzu Corporation [2]. Now the camera is available in market. The very high performance has been proved through applications of the camera to various targets in scientific and engineering research and development.

Fig. 4 shows example images of a shock wave reflected at and transferred through a water surface captured at 500,000 fps. Sound in water propagates much faster than in air as learned from textbooks.

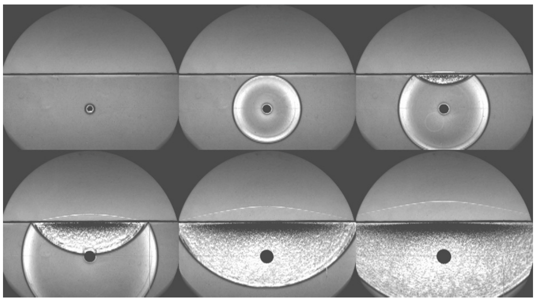


Fig. 4 Shock wave propagation at a water surface. (Captured by Takayama et al with the ISIS-V2 at 500,000 fps)

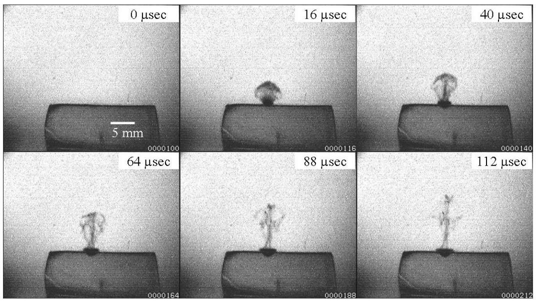


Fig. 5 Laser ablation of gelatin (10 wt%; water 90 wt%). (Captured with the ISIS-V2 at 250,000 fps)

Fig. 5 shows ablation from gelatin by a shot of a pulsed laser beam captured at 250,000 fps [5]. The wave length, the pulse width and the energy density of the beam are 10.6 microns, 80 ns and 6.7 J/cm$^2$, respectively.

## 2.4 Evolution of the ISIS

The ISIS-V2 is a monochrome sensor with the pixel count of only 81,120 (= 312 × 260). The color version with higher resolution with the pixel count of 302,400 (= 420 × 720) has been developed by NHK (Ohtake, Hayashida *et al.*, 2006) [6]. The ISIS is continuously being evolved. As shown in the following sections, currently, the ISIS-V12 with ultra-high sensitivity as well as ultra-high frame rate is under processing, and the ISIS-16M, aiming at 16 Mfps at first and 100 Mfps in the future, is being designed with sacrifice of the dynamic range.

The ISIS concept has been applied to develop novel high-speed image sensors in other organizations. For example, in the LCFI, the linear collider flavour identification, a group of scientists are developing a new sensor based on the concept (Allport *et al.*, 2005, Stefanov, 2006) [7, 8]. They employed the CMOS readout scheme combined with the ISIS for the storage part for more flexible readout after capturing a signal sequence. The combination was proposed by the authors in 2002 (Etoh *et al.*, 2002) [9] and named RA-ISIS, the random-access in-situ storage image sensor.

The evolution process is summarized in Table 1. Example images of the ISIS-V4, the color and high-resolution version of the ISIS, are shown in Fig. 6.

# 3. PC-ISIS: Image Sensor with Ultra-High Speed and Ultra-High Sensitivity

## 3.1 The PC-ISIS

### 3.1.1 Combined technologies

The ISIS achieved ultra-high speed image capturing up to 1 Mfps. For microscopic observation, ultra-high sen-

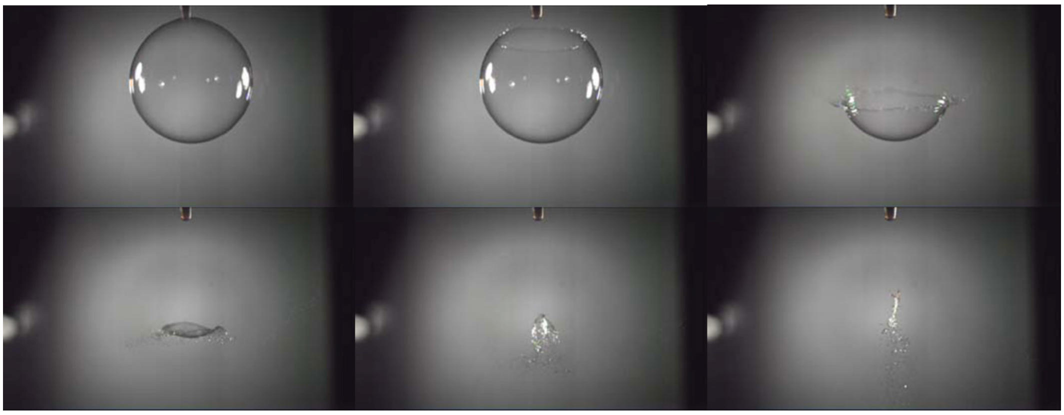


Fig. 6 A soap bubble (Captured with the ISIS-V4 at 5,000 fps).

Table 1 The evolution of high-speed image sensors in Kinki University and NHK.

| **Sensor / Camera** | **Parallel and partial readout sensor** | **ISIS** | | | |
|---|---|---|---|---|---|
| | | **Frontside illuminated** | | **Backside illuminated** | |
| | **Photron FASTCAM / KODAK EKTAPRO HS4540** | **ISIS-V2** | **ISIS-V4** | **ISIS-V12** | **ISIS-16M** |
| **Pixel count (pixels)** | 65,536 (256x256) | 81,120 (312x260) | 302,400 (420x720) | 201,600 (480x420) | 172,800 (480x360) |
| **Maximum frame rate** | 4,500 fps for full frame (40,500 fps for 64x64 pixels) | 1 Mfps | 1 Mfps | > 1 Mfps | > 10 Mfps |
| **Device for high sensitivity** | MCP | | | CCM / Backside illumination / Cooling | |

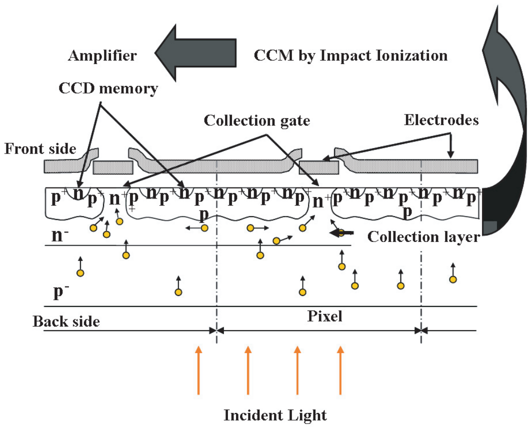


Fig. 7 PC-ISIS: the cross section ①-①’ in Fig. 1.

sitivity is also required. The sensitivity of less than 10 photons will be achieved by introduction of three existing technologies: backside-illumination, cooling, and the CCM, Charge Carrier Multiplication invented by Hynecek (1993) [10].

The sensor under development satisfies both requirements of the ultra-high speed and the ultra-high sensitivity. The sensor was named the PC-ISIS, the Photon-Counting In-situ Storage Image Sensor.

### 3.1.2 Cross-section structure

The cross section ①-①’ in Fig. 1 is shown in Fig. 7. The ISIS structure and the CCM are installed on the surface of the PC-ISIS. Therefore, the structure of the PC-ISIS is much more complex than that of the standard backside illuminated CCD. In this figure, arrows express flow of electrons.

In the figure,

(1) Electron-hole pairs are generated in the backside layer by the incident light to the backside of the sensor.

(2) The electrons are transferred to the collection gates through the collection layer, and stored as image signals in the linear CCD channels, which run perpendicularly to the paper surface.

(3) The holes are continuously drained from the sensor.

## 3.2 Pixel structure

The specifications of the pixel and the sensor are summarized as follows:

(1) Pixel Size

The length of a CCD cell is 3.6 $\mu$m. Each pixel consists of ten CCD channels, the collection gate and drains for holes and electrons. Each CCD channel has twelve CCD cells. The size of a pixel is the product of the size and the number of CCD cells in one channel, i.e., 3.6 $\mu$m $\times$ 12 elements = 43.2 $\mu$m.

(2) Thickness of the chip

To achieve fast electron transfer, the sensor should be completely depleted. Therefore, thinning process is applied to the chip to 24 micron thick.

(3) Pixel count and the size of the chip

The pixel count is 172,800 pixel (480 × 360). The size of the photo-receptive area is 20.73 × 15.552 mm$^2$, calculated by multiplying the pixel size and the pixel count.

(4) Number of frames

The number of frames of continuously captured image is 117, which is the same as the number of the CCD storage elements for one pixel.

(5) Sensitivity

With combination of the 100% fill factor by backside illumination and the amplification by impact ionization (CCM), the sensitivity is expected to be less than 10 photons for standard readout rate.

Since the PC-ISIS is a backside-illuminated image sensor, it is sensitive to ultraviolet rays and visible light.

On the other hand, infrared ray and some portion of red light penetrate through the 24-micron-thick chip and reach the CCD storage channel made on the surface. Therefore, the sensitive wave length of the sensor is limited up to 600 nm.

(6) Other functions

Overwriting mechanism is installed. Continuous parallel readout is also possible up to 500 fps.

# 4. Further Increase of the Frame Rate

## 4.1 CCD element structure

The authors have started the design of the PC-ISIS operating at 16 Mfps, and finally at 100 Mfps. However, the charge handling capacity of the CCD element decreases, which results in the lower dynamic range.

Fig. 8 shows the plane structure of the CCD element.

## 4.2 Sensor structure

Fig. 9 shows the plane structure of the sensor. It has four independent blocks, each with a photo-receptive area, a readout CCD, a CCM, an amplifier and a readout tap. The driving voltage is delivered both from the top and the bottom edges of the sensor.

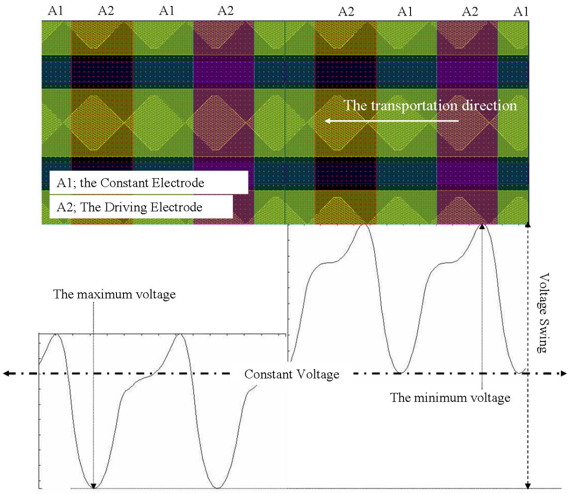


Fig. 8 The plane structure of the new CCD elements.

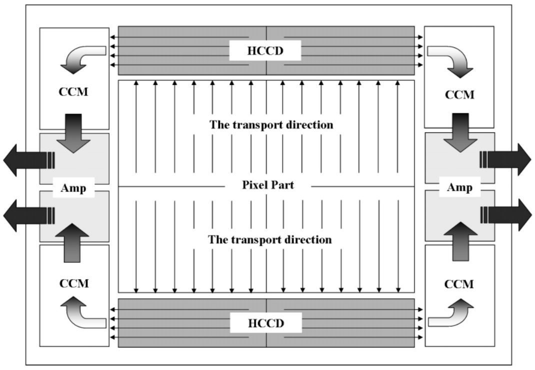


Fig. 9 The plane structure of the sensor.

## 4.3 Preliminary simulations

### 4.3.1 Transfer in the collection layer and the theoretical maximum frame rate

Preliminary simulations are conducted by using the parameters shown in Table 2.

The frame rate is the inverse of the time for an electron to travel from the edge of a pixel to the collection gate through the collection layer, and finally to the input gate. Along the electron path, sufficiently smooth electric field must be realized, as shown in Fig. 10. Even if there is a slight up-and-down or a long flat root in the path, electrons are trapped or detained, which causes serious decrease of the traveling time. To achieve the maximum frame rate, the minimum electric potential gradient (electric field) in the path should be maximized. Extensive simulation study for the pixel of $43.2 \times 43.2\,\mu\text{m}^2$ and the thickness of 24 μm has finally realized that the traveling time through the collection layer is 5.6 ns and that in the collection gate is 0.9 ns; the total is less than 6.5 ns. Therefore, the theoretical maximum frame rate of this sensor is expected to be more than 100,000,000 fps.

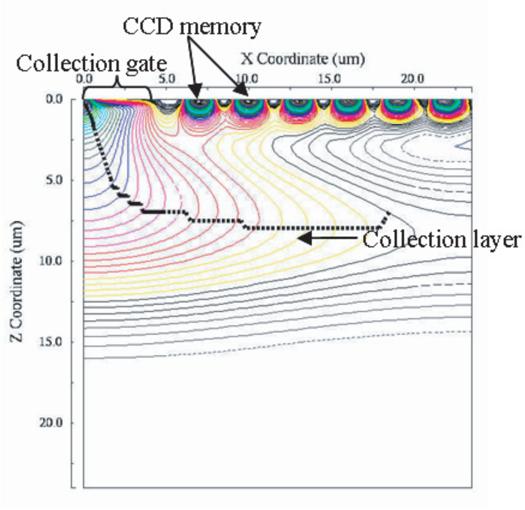


Fig. 10 An example of the electric field and the electron path in the X-Z section of the PC-ISIS.

Table 2 The parameters and results of the preliminary simulation.

| Parameters | Transfer system | | |
|---|---|---|---|
| | Four-phase | Single-phase | Two-phase |
| Channel width ( μm ) | 3.0 | 3.0 | 3.0 |
| A CCD element ( $\mu m^2$) | 3.0 x 3.6 | 3.0 x 3.6 | 3.0 x 3.6 |
| The size of an electrode ( $\mu m^2$) | 3.0 x 0.9 | 3.0 x 1.8 | 3.0 x 1.8 |
| The size of pocket for the area for a charge packet ( $\mu m^2$) | 3.0 x 1.8 | 3.0 x 0.9 | 3.0 x 0.9 |
| The swing voltage ( V ) | 10 | 14 | 7 |
| Charge handling capacity ( e- ) | 24000 | 3000 | 5000 |

#### 4.3.2 Channel potential and charge handling capacity

Preliminary simulations are also conducted to optimize the channel potential profile and estimate the charge handling capacity. The charge handling capacity was so far estimated as 3,000 e- for the virtual transfer system and 5,000 e- for the standard two phase transfer system, respectively.

## 5. Sensor with a Large Area

### 5.1 Technologies to produce large sensors

The ISIS has very large pixels, since many storage elements are installed in each pixel, resulting in the relatively small pixel count. Therefore, to increase the spatial resolution of the ISIS, it is required to enlarge the size.

Large image sensors are also required in various scientific and engineering fields for higher spatial resolution. For example, a standard window size of a TEM is much wider than that of the standard image sensors.

Currently, there are three technologies available to make large-area image sensors as follows: (1) Stitching, (2) Butting, and (3) Overlapping.

Stitching connects the mask images on a wafer to make an IC chip with a large area. The yield rate of an IC device decreases inversely proportionate to the third to the forth power of the area. Since the chip is processed and diced as one large sensor after stitching on the wafer, the yield rate seriously drops for increasing the area.

Butting pastes medium-size chips on a surface of a package with very small gaps. It has been applied to large-size sensors for astronomy. Usually, one column and/or row between adjacent chips is lost. Fortunately, since the pixel size of the ISIS is very large, butting was successfully applied to the ISIS-V4 to double the pixel count from 420 × 360 to 420 × 720 as shown in Fig. 11 (Ohtake, Hayashida *et al.*, 2006) [6].

An example of overlapping technology is shown in Fig. 12. This is “The Terraced Image Sensor” proposed by Etoh *et al.* (2002) [11]. The narrow open area of each chip receives the incident light and the other area is used for memories and image signal processing, such as ADC.

### 5.2 Precision dicing close to the photodiode

To make butting sensors and terraced image sensors, the wafer should be diced very close to the photodiodes.

Fig. 13 shows the diced cross section. The dicing angle is slightly larger than 90 degrees for perfect butting. A special dicing machine with slanted saw was introduced. Otherwise, the bottom edges of the chips contact and the top edges have some opening by automatically slightly

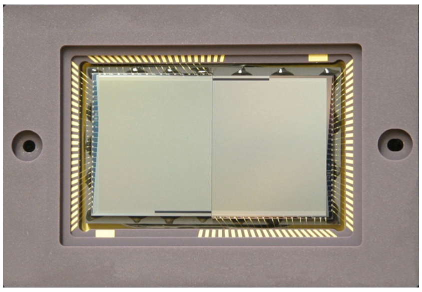


Fig. 11 ISIS-V4 made by butting [6].

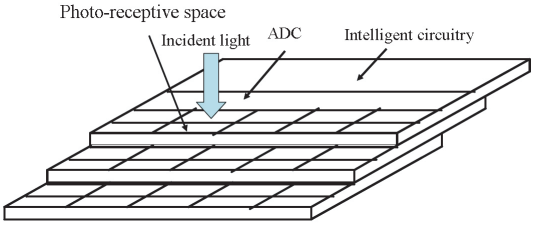


Fig. 12 Terraced image sensor.

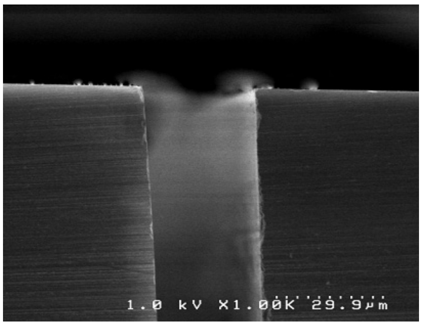
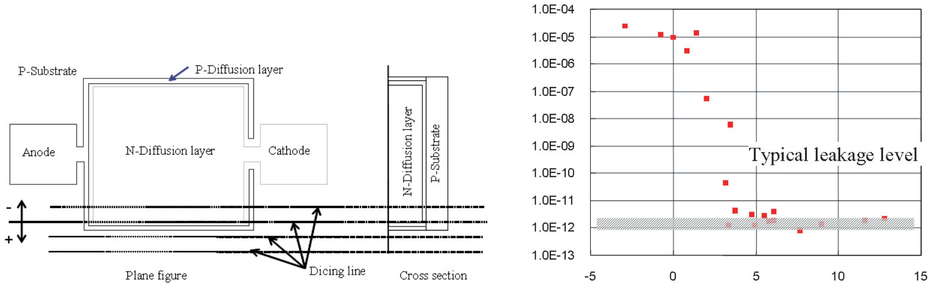


Fig. 13 Dicing with a small angle [6].



(a) Dicing lines (b) Leakage

Fig. 14 Leak current vs. distance between a dicing line and a diode (After Ohtake, Hayashida *et al*. [6]).

slanting dicing saw of the standard dicing machine.

Fig. 14 shows the leak current due to dicing very close to a diode (Ohtake, Hayashida *et al.*, 2006) [6]. If the distance from the edge of the photodiode is larger than 3 $\mu$m, no leakage appears practically. The critical distance is possibly decreased by removing the surface of the dicing face from which micro cracks may have developed to the depth of three microns.

## 5.3 Focusing for the terraced image sensor

Fig. 16 shows the results of experiments on the depth of focus on two terraced chips with the thickness of 50 $\mu$m.

Commonly, the depth of field is expressed as

$$D = 2 \times (\text{F-value of the optical system}) \times (\text{pixel size})$$

Generally, if the thickness T of the chip is less than 2D, the incident light image focuses on both of the chip surfaces.

For the experiments, a video camera with a progressive CCD image sensor with 1,000 × 1,000 pixels of the CCD element size of $9.0 \times 9.0\,\mu\text{m}^2$ is applied. The F-value is 1.4. Therefore, the depth of field D is 25.2 $\mu$m ($= 2 \times 1.4 \times 9$).

The test pattern is shown in Fig. 15.

In the experiments, the camera was slid from the position of the perfect focusing. Fig. 16 shows the perfectly focused images in the upper half of the frame and the defocused ones in the lower half.

The result showed that if the defocusing distance is less than 100.8 $\mu$m, i.e., the thickness T is less than 4D, defocusing is negligible, which suggests that the terraced

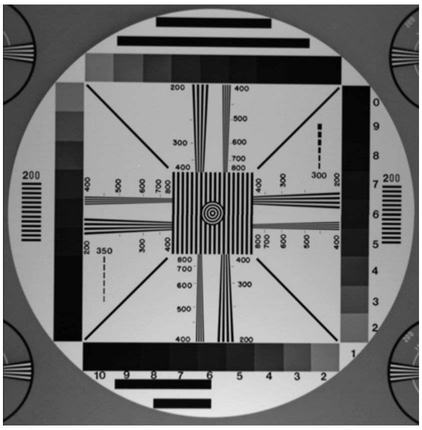
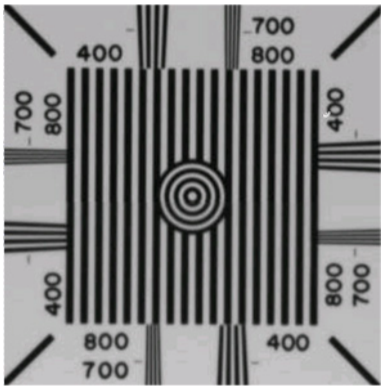
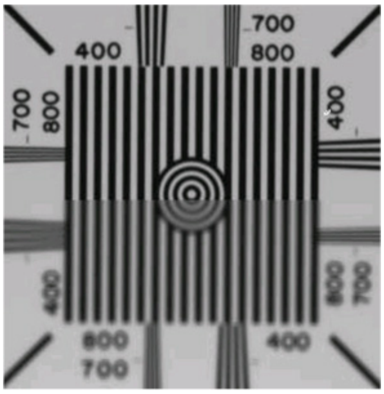


Fig. 15 The test pattern.



(a) T=4D=100.8 $\mu$m



(b) T=8D=201.6 $\mu$m

Fig. 16 Evaluation of defocusing on the terraced image sensor.

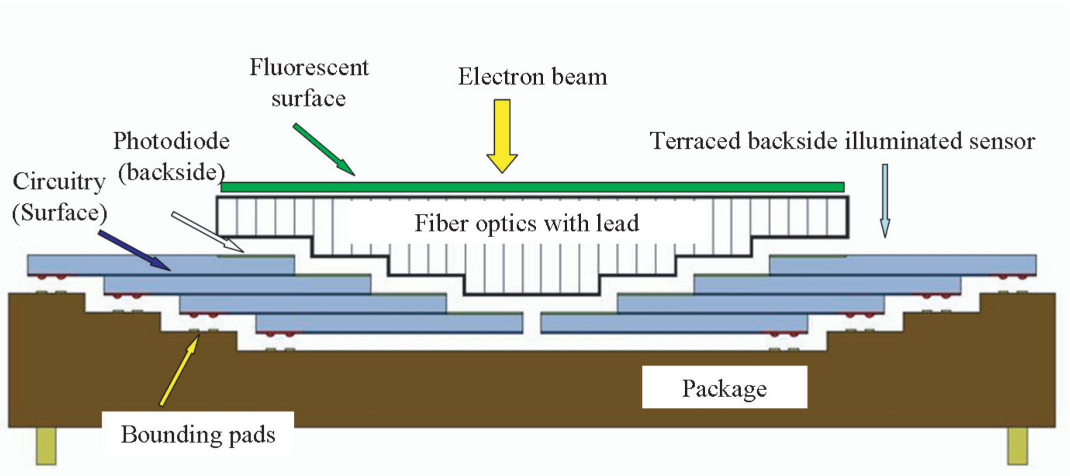


Fig. 17 Terraced image sensor for Dynamic TEM.

image sensor is practical.

Fig. 17 proposes a terraced image sensor for the TEM. The terraced surface is covered with fiber-optics with stepped bottom surface and the flat top surface. The fiber is made of glass doped with thick lead to prevent the CCD from damage due to X rays.

## 6. Conclusion

Since the early 1990's, the authors have been engaged in development of high-speed video cameras. This paper summarized the evolution process in the past and the perspective of the future development.

The maximum frame rate of the currently available cameras is 1 Mfps. Design of the new sensor aiming at 100 Mfps in the future has started.

To achieve 100 Mfps, other supporting technologies should be developed in parallel, which includes a special power circuitry.

The authors sincerely hopes our ultra-high-speed video cameras will contribute to research and development on the plasma physics and engineering.

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